Rapid Learning in High Velocity Environments

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Rapid Learning in High Velocity Environments

This dissertation investigates how rapid learning occurs in high technology industries, many of which operate in what Bourgeois and Eisenhardt (1988)[i] term "high velocity environments." The dissertation consists of three empirical studies, which follow the method of extended case study research (e.g. Yin, 1981; Eisenhardt, 1989a).[ii] Semiconductor manufacturing and process development are chosen as settings for this dissertation because they exemplify most of the attributes of high velocity environments.[iii] Data for the three studies come from 69 cases of organizational learning that transpired in 35 factories and laboratories across Asia, Europe and North America. The cases were divulged in interviews with 37 respondents. They are supported by large, quantitative data sets, which have been published in the semiconductor industry's technical literature.[iv] An additional series of interviews, which solicit the expertise of 61 specialists in a variety of disciplines that pertain to semiconductor manufacturing, is conducted to drive the propositions and models in this dissertation into theoretical saturation. Experts for these interviews are recruited by recommendations from within their respective peer groups.

The first study looks into how firms organize for learning. Existing definitions of modularity (McClelland & Rumelhart, 1995[v]; Ulrich, 1995[vi]; Baldwin & Clark, 1997[vii]) are expanded to provide a theoretical framework for differentiation and integration of organizations (Lawrence & Lorsch[viii]), technology (Iansiti & West[ix]), learning activity, accumulated knowledge and performance metrics in high velocity environments. The results of the study imply that organizational differentiation in high velocity environments occurs with a high degree of modularity (the individual modules exhibit little interdependence), which fosters learning efficiency. The high level of modularity is observed in multiple distinct categories such as learning activities, knowledge bases, organizational structure and performance metrics (figure 1).

The results from study #1 indicate that complex design rules mandate an extraordinary integration effort, which requires specialized integration knowledge and manifests itself in the form of a clearly identifiable integrating device (figure 1, row c). Evidence suggests that the design rules for organizational functions are relatively straightforward -- in 33 of the 35 work environments under study they break down the manner illustrated in figure 2. Subsystem metrics uniquely characterize the learning efforts of organizational subsystems. Subsystem metrics are converted to performance factors, which are multiplied to determine the performance of the organization.[x] No integrating devices for integration of organizational functions were deemed necessary, and none could be identified in any work environment – the integration of functions generally occurs through ad hoc mechanisms.[xi] By contrast, the design rules for technological subsystems in semiconductor manufacturing are significantly more complicated: documenting the explicit knowledge that is required to generate a set of semiconductor design rules typically cannot be achieved in less than 50 pages of printed text. Integrating devices for integrating the constituent technologies of a semiconductor process (yield groups in manufacturing or process integration groups in R&D) were technology were identified in 29 out of 35 work environments under study.[xii]

Study #1 demonstrates that the modularity of relationships between categories (figure 3) can influence organizational structure. A one-to-one mapping between categories resulted in total organizational differentiation in all of the 35 work environments under study, whereas a many-to-many mapping tended to prevent total differentiation (figure 4). All work environments under study were first differentiated by function and subsequently by technology. Relationship modularity was inherited with differentiation in all instances (figure 5).

The second study explores the inner mechanisms of rapid learning, by building an empirically grounded[xiii] model of the lifecycle of a semiconductor manufacturing process (figure 6), whose structure resembles figure 5. Study #2 leads to the conclusion that learning in high velocity environments is *leveraged*: prolonged, sustained, relatively constant investments in learning at the subsystem level generate punctuated surges in performance at the organization level. Three causes of learning leverage have been identified: 1) the practice of solving problems in decreasing order of perceived impact – i.e. by applying the Pareto Principle (Juran, 1974);[xiv] 2) highly non-linear relationships between subsystem metrics and performance factors[xv]; and 3) the practice of using a multiplicative model to integrate performance factors. [x]

Study #2 shows that organizational learning proceeds according to Liebig's Law of the Minimum.[xvi] Performance at the organization-level is proportional to the performance of its most limiting performance factor. Weakly performing subsystems constrain and delay performance at the organizational level, in addition to diminishing the contributions to global organizational performance of relatively well-performing subsystems. Management focuses on the weakest performance factor until that factor is no longer the weakest one, and shifts attention to the mechanism that replaces it as the weakest one. Knowledge that resides within well-performing subsystems is hidden from the upper management of organizations that primarily evaluate their performance through global, organization-level metrics (figure 7).

The third study investigates the effects of learning leverage on the profitability of a firm that is under time-to-market pressure. In this study, a realistic profile of product unit price erosion is incorporated into the model from study #2. The enhanced model [xiii] presents evidence that a prolonged, sustained investment in learning at a relatively constant level generate highly non-linear surges in revenue, but financial performance deteriorates as market windows draw to a close (figure 8). On balance learning how to generate revenue is significantly more important than learning to reduce unit cost.[xvii]

Analysis of the model indicates that a slight, but coordinated acceleration of the organizational learning rate enhances profitability more than any other factor does (figure 9). Factors such as maximizing product quality (process learning), increasing scale (production learning) or reducing a product's susceptibility to quality problems (design learning) are subordinate and reach diminishing returns. The finite capabilities of suppliers prevent semiconductor manufacturers from accelerating their learning efforts ad infinitum. If the timing of a market window is known well in advance,[xviii] then an organization can orchestrate a "learning coup" by coordinating subsystem learning efforts in a manner that causes organization-level performance to surge just before the market window opens.

Study #3 concludes that semiconductor ventures are highly vulnerable to environmental shifts,[xix] which manifest themselves in the form of changes in the rate of product unit price erosion. However, a select few semiconductor manufacturers are in a position to increase a semiconductor manufacturing venture's profitability by delaying product unit price erosion through the exercise of *platform leadership* (Gawer & Cusumano, 2002[xx]), a capability that is becoming increasingly important because market windows have eroded from an average duration of 4 years in the 1990s to a duration of less than 6 months in 2003.[xxi]

Study #3 indicates that rapid learning in high velocity environments is a complex coordination problem requiring a high level of management skills in human resources, technology and finance. The requisite management skills in this high-wire feat are sufficiently rare, so as to comprise a significant barrier to entry. The key to success appears to come from managing intangibles and through predicting from existing knowledge problems that are likely to occur and designing mechanisms for their rapid solution before they occur.

In conjunction, the three empirical studies in this dissertation lay the foundation for a normative, *metrics-driven*, pragmatic[xxii] theory of learning. The theory recommends that firms execute the following sequence of steps to enhance their potential for rapid learning in high velocity environments.

1) ***Define the global objective*** of a venture and select the global metrics that best measure whether the venture is making progress towards its stated objective.

2) ***Build a learning architecture*** that supports the global objective of the venture, i.e. define a hierarchy the metrics that allow the firm to achieve the objective in the most effective manner. (See, for example, figure 10.)

3) ***Organize for learning*** by defining a hierarchy of activities that are aligned with the metrics of the learning architecture. Match organizational structure to this hierarchy of activities.

4) ***Manage according to Liebig's Law of the Minimum.*** If the timing of the market window is known well in advance,[xviii] then orchestrate a "learning coup".

5) ***Prepare for change*** before change occurs, by spreading knowledge as rapidly as possible throughout the organization.[xxiii]

Interviews with 15 practitioners from outside the semiconductor industry suggest that the theory developed in this dissertation can, in principle, be extended to other industries within or outside high technology or high velocity environments.

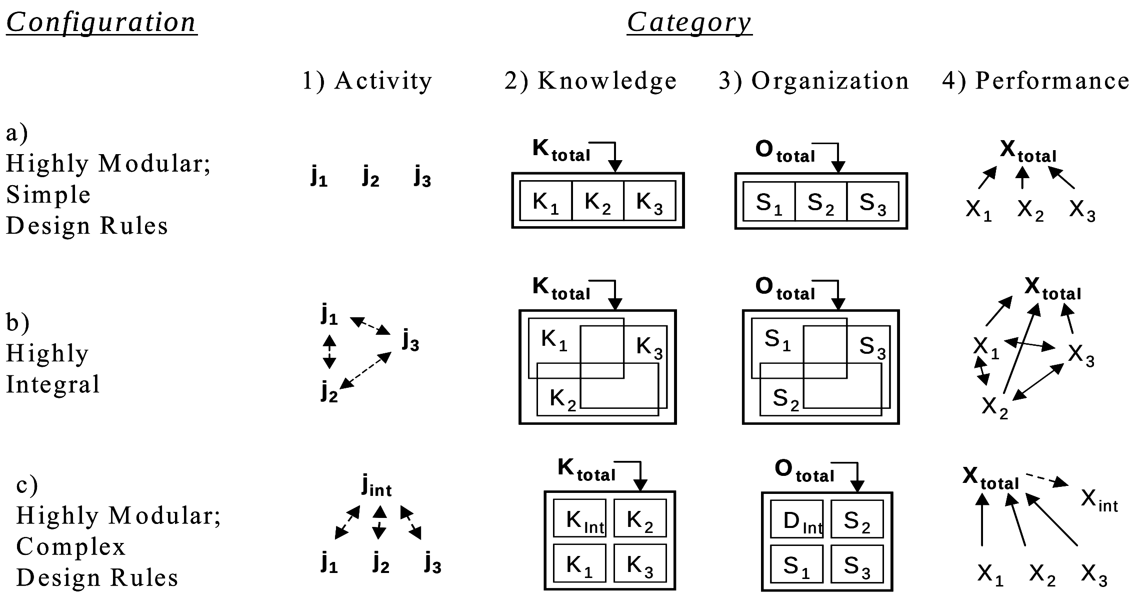

Figure 1: **Illustration of 1) activity modularity, 2) knowledge modularity, 3) organizational modularity and 4) performance modularity in a) a highly modular organizational learning endeavor with simple design rules, b) in a highly integral organizational learning endeavor and c) in a highly modular organizational learning endeavor with complex design rules. The letters j_1, j_2 and j_3 denote distinct activities that need to be integrated by an activity j_{int}, if the design rules of the system are complex. K_{total} depicts a knowledge base that consists of subordinate knowledge bases K_1, K_2, K_3 and an optional knowledge base for integration K_{int}; O_{total} represents an organization that consists of three subsystems – S_1, S_2, S_3 – and an optional integrating device D_{int}. Unidirectional arrows indicate directional dependence. Bidirectional arrows indicate interdependence. X_{total} denotes the performance metric of a system that depends upon the performance metrics of X_1, X_2 and X_3. X_{int} denotes integration performance, which is covered by X_{total}, but not by X_1, X_2 or X_3.**

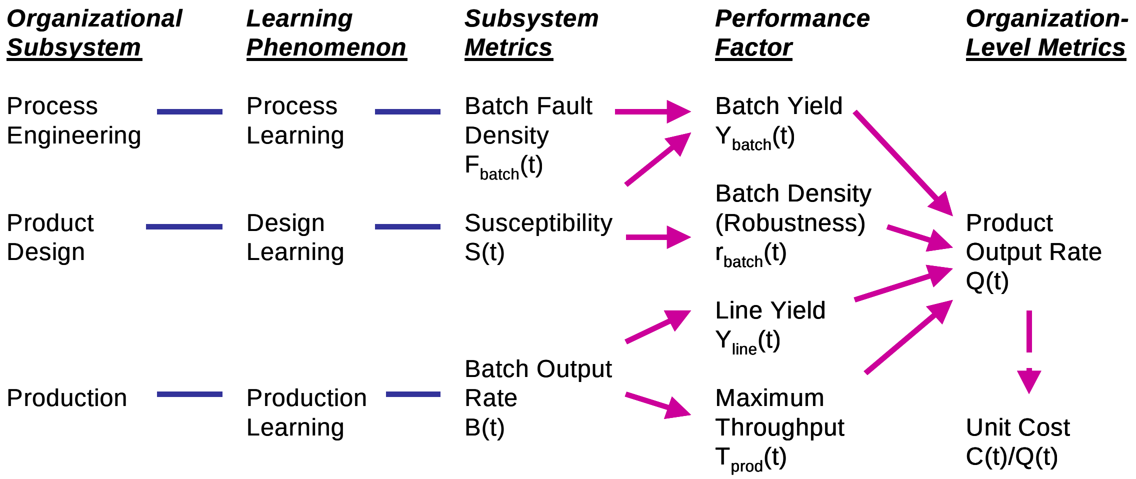

Figure 2: **Structure of organizational learning in semiconductor manufacturing organizations.**

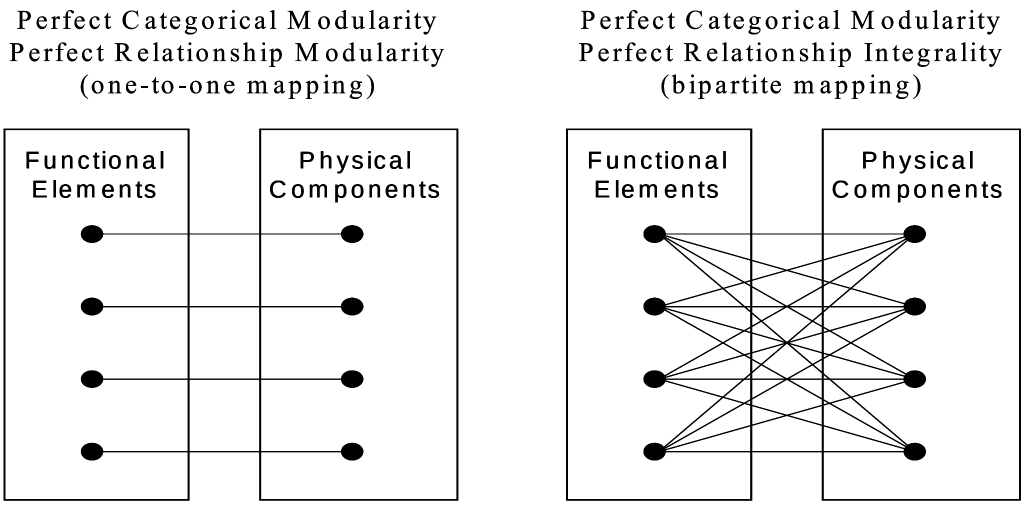

Figure 3: **The relationship between the functional elements and the physical components of a product design can exhibit relationship modularity or relationship integrality (modeled after Ulrich, 1995).**[vi] **(The** *categorical modularity* **of a system is defined as the degree to which the elements of the system can be classified into categories without having elements of the system be members of more than one category.)**

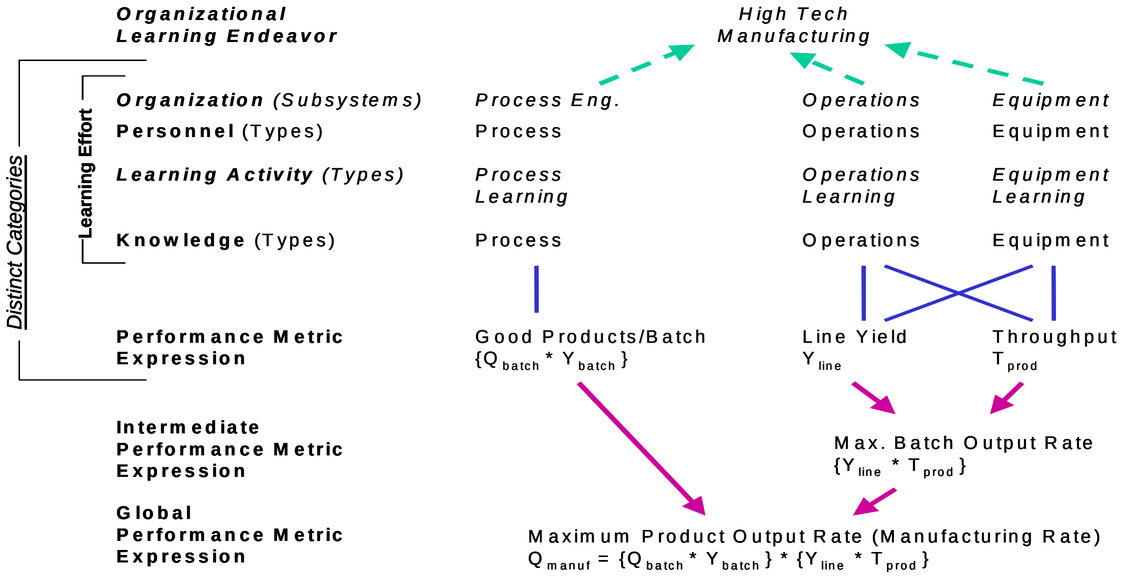

Figure 4: **Differentiation of an organizational learning endeavor in a high technology manufacturing environment. Three distinct learning efforts are mapped onto three distinct performance metrics. The process engineering effort maps one-to-one with good products per batch; the operations and equipment efforts map many-to-many with line yield and throughput. Process engineering subsystems did not overlap with operations or equipment subsystems in any of the 35 work environments under study. However, the operations and equipment subsystems tended to overlap or be indistinguishable in more than 80% of all work environments, even though distinct skill sets (operations and equipment) could be identified.**

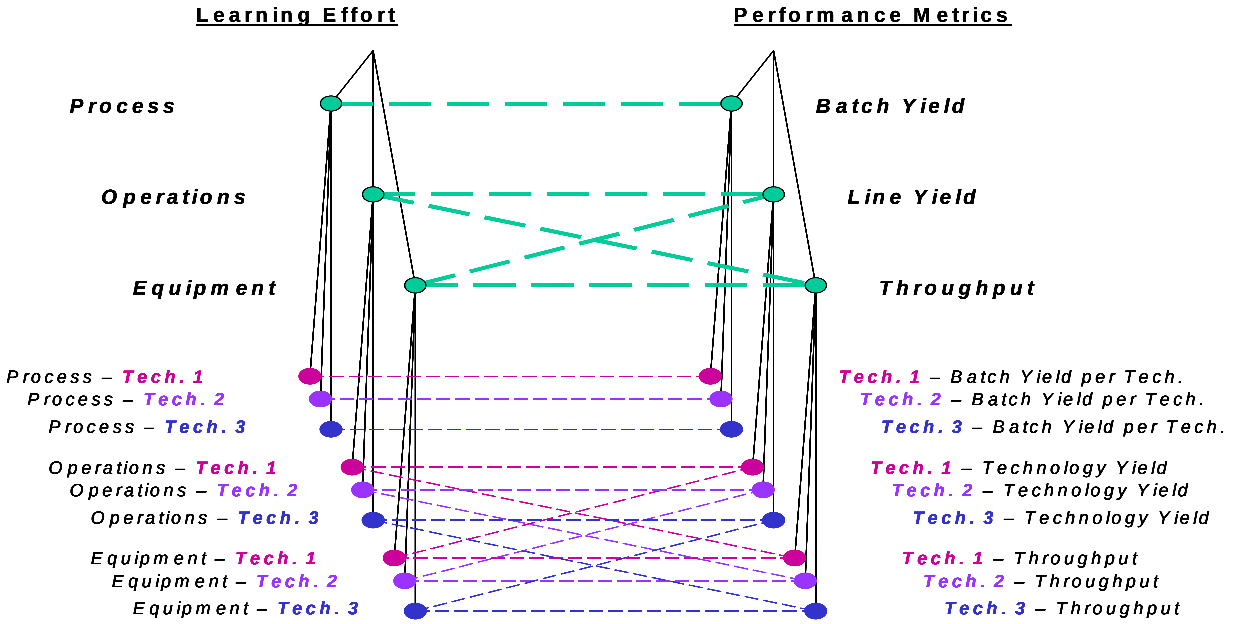

Figure 5: **Differentiating a learning endeavor first by function and subsequently by technology. Relationship modularity is inherited with differentiation.**

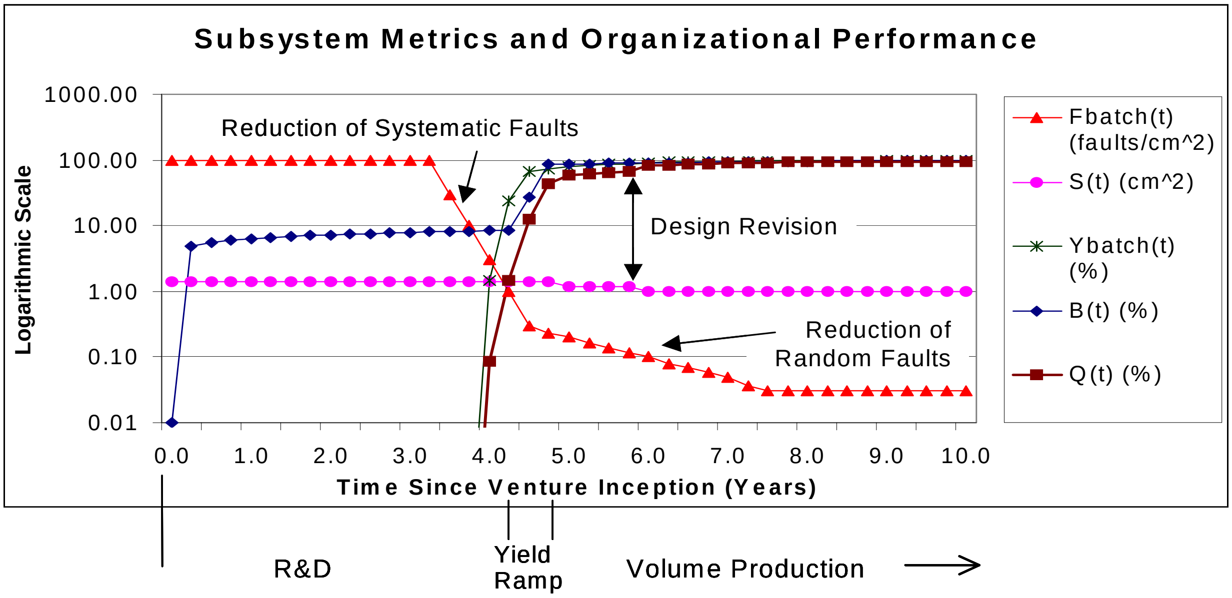

Figure 6: **The behavior of subsystem metrics in figure 2 and the organization-level metric Q(t) over a 10-year semiconductor process lifecycle is depicted on a semi-logarithmic scale. Batch yield, a performance factor, is included to illustrate the exceptional learning leverage that can be obtained from process learning. Process learning results in an exponential reduction of batch fault density, which causes a surge in batch yield that triggers the Yield Ramp, a period of intense production learning in which batch yield and batch output rate rise simultaneously.[xxiv] Production learning and design learning dominate during volume production, when process learning exhibits low leverage.**

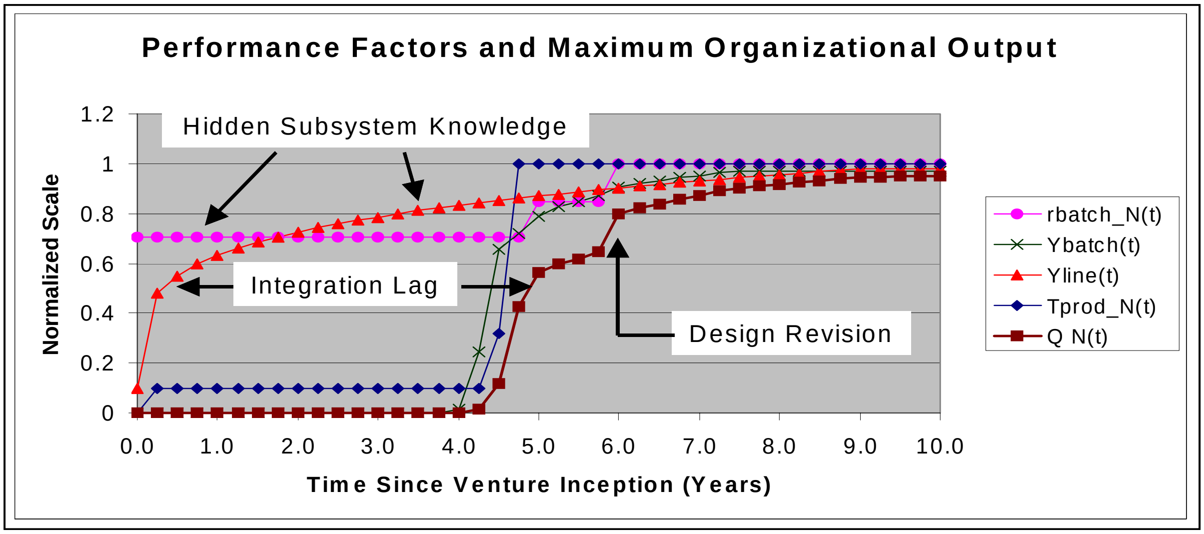

Figure 7: The behavior of performance factors and the organization-level metric $Q_N(t)$ throughout a semiconductor lifecycle is depicted on a normalized scale.[xxv] The total manufacturing rate $Q_N(t)$ rises to appreciable levels more than four years after a line-yield competency is established. Production knowledge that generates line yield is hidden from organization-level performance metrics, which are constrained and disproportionately impacted by batch yield, a performance factor of the relatively weakly performing process engineering subsystem. A commonly observed design revision, which occurs about six years into the semiconductor process lifecycle, causes a surge in robustness of a design ($r_{batch\_N}(t)$). Learning leverage, which is derived from the highly non-linear relationship between batch yield and susceptibility to faults, amplifies the impact on $Q_N(t)$.

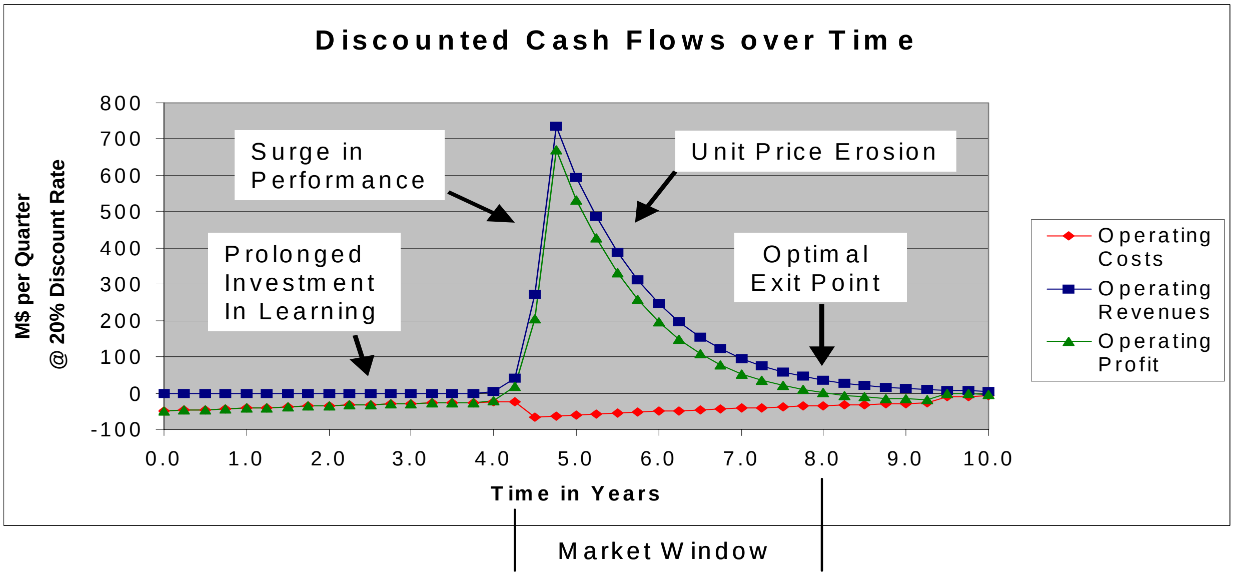

Figure 8: **Learning leverage under time-to-market pressure. During the early stages of production learning how to generate revenue is more important than learning how to reduce cost. Learning how to reduce unit cost becomes important shortly before the market window closes. Total-cost-of-ownership models,[xxvi] which have been customized for semiconductor manufacturing, determine operating costs.**

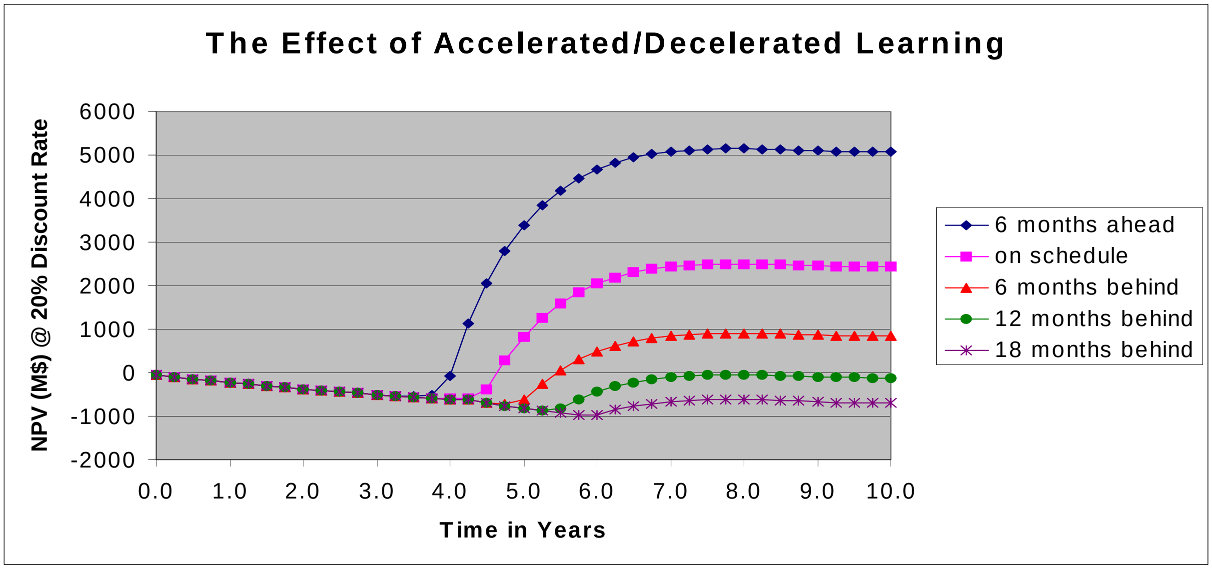

Figure 9: **How much you learn, may be less important than when you learn it. Accelerating the process-learning rate by 6 months doubles the maximum NPV[xxvii] of a semiconductor venture; accelerating the schedule beyond that limit exceeds the capabilities of suppliers. Being 12 months behind schedule wipes out all profit. (The schedule in figure 9 is benchmarked with respect to Moore's Law.[xviii])**

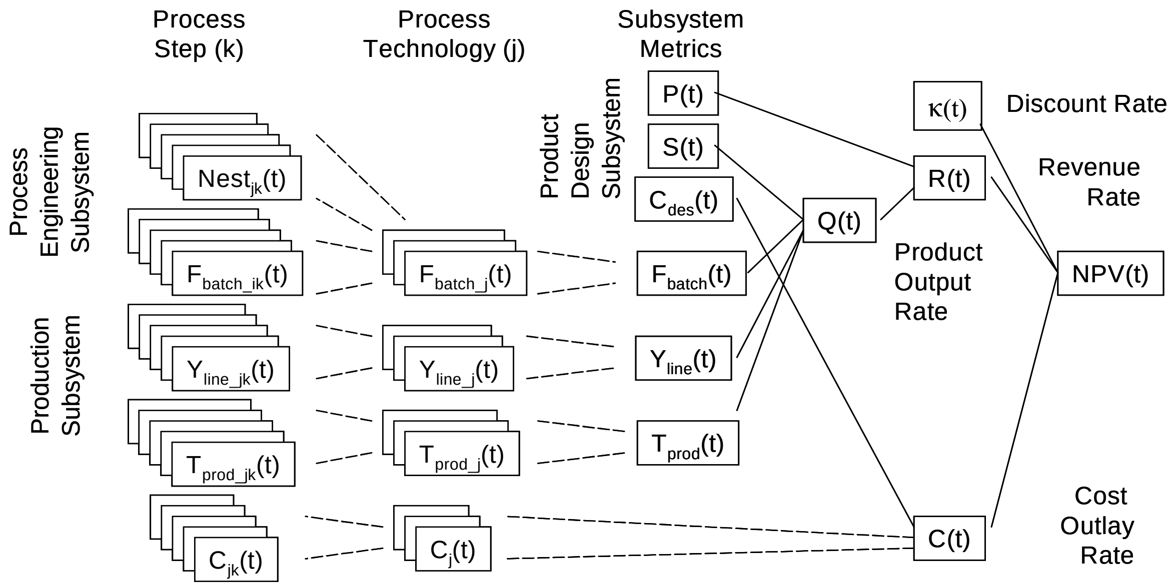

Figure 10: **Learning architecture for semiconductor manufacturing that is consistent with total quality control procedures (Deming, 1982).[xxviii] Explanation of parameters: t ➔ time since venture inception; Nest(t) ➔ nesting factors; $F_{batch}(t)$ ➔ batch fault density; $Y_{line}(t)$ ➔line yield; $T_{prod}(t)$ ➔ maximum production throughput; P(t) ➔ unit price of design; S(t) ➔ design's susceptibility to faults; Q(t) ➔ maximum product output rate; C(t) ➔ Cost outlay rate as determined by cost of ownership models; R(t) ➔ revenue generation rate; κ(t) ➔discount rate (opportunity cost of capital); NPV(t) ➔ net present value. The letters "j" and "k" respectively act as identifiers of process technologies and individual process steps.**

References

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[i] Eisenhardt, Kathleen M. and L. J. Bourgeois III. “Politics of Strategic Decision Making in High-Velocity Environments: Toward a Midrange Theory.” *Academy of Management Journal*, 1988, Vol. 31, No. 4, 737-770.

[ii] Yin, Robert K., “The Case Study Crisis: Some Answers,” *Administrative Science Quarter*ly, March 1981, volume 26, pp. 58-65; -- K. M. Eisenhardt, "Building theories from case study research," *Academy of Management Review*, Vol. 16 (1989), pp. 620-627.

[iii] High technology manufacturing and process development tend to be yield driven {R. E. Bohn and C. Terwiesch (1999), "The Economics of Yield-Driven Processes," *Journal of Operations Management* 18(1), pp. 41-59.}; they can occur prior to product release {Pisano, Gary P., "Learning before doing in the development of new process technology," *Research Policy* 25 (1996), pp. 1097-1119.}; they may include substantial engineering efforts {P.S. Adler, and K. B. Clark (1991), "Behind the learning curve: A sketch of the learning process," *Management Science*, 37, 3, 267-281}; and may require “learning how to learn” {W. Hirsch, "Firm progress ratios," *Econometrica*, Vol. 24 (April 1956), pp. 136-144; -- W. Fellner, “Specific Interpretations of Leaning by Doing,” *Journal of Economic Theory*, Aug., 1969, 1, pp. 119-140; -- L. Dudley, “Learning and productivity change in metal products,” *The American Economic Review*, Vol. 62, Issue 4 (Sept., 1972), pp. 662-669.}. Calendar time, rather than cumulative output, serves as a superior proxy for the learning investment in high velocity environments.

[iv] These include R. C. Leachman, "Competitive manufacturing survey: third report on the results of the main phase," *UC Berkeley Report CSM-31*, University of California, Berkeley, 1996; -- R. C. Leachman and D. A. Hodges (1996), “Benchmarking Semiconductor Manufacturing,” *IEEE Trans. Semicond. Manufact*., Vol. 9, no. 2, pp. 158-1169, May 1996; -- C. Stapper and R. Rosner, “Integrated circuit yield management and yield analysis: Development and Implementation,” *IEEE Trans. Semicond. Manufact*., Vol. 8, no. 2, pp. 95-101, May 1995; -- C. Weber, B. Moslehi and M. Dutta, “An integrated framework for yield management and defect/fault reduction,” *IEEE Trans. Semicond. Manufact*., Vol. 8, no. 2, pp. 110-120, May 1995; -- Semiconductor Industry Association, *The (Inter)national Technology Roadmap for Semiconductors,* 1994, 1997, 1999, 2001.

[v] A module is defined as a unit whose structural elements are powerfully connected amongst themselves and relatively weakly connected to elements in other units. A system that exhibits strong connections within modules and weak connections between modules is considered a highly *modular* system. A system that exhibits relatively weak connections within modules and relatively strong connections between modules is considered an *integral* system. {McClelland, J. L. & D. E. Rumelhart (1995), *Parallel Distributed Processing*, Cambridge, Mass., MIT Press.}

[vi] A modular product architecture is defined as one that “includes a one-to-one mapping from functional elements in the function structure to the physical components of the product, and specifies de-coupled interfaces between components.” {Ulrich, K. T. (1995), “The role of product architecture in the manufacturing firm,” *Research Policy* 24: p. 422.}

[vii] Modular systems are composed of units (modules), which are designed independently but still function as an integrated whole. Designers achieve modularity by partitioning information into visible design rules and hidden design parameters that do not affect the design beyond the local module. Visible *design rules* specify what modules will be part of the system and what their functions will be; *interfaces* describe in detail how the modules fit together and how they will interact. {Baldwin, Carliss Y. and Kim B. Clark (1997), "Managing In An Age of Modularity", *Harvard Business Review*, Vol. 75, No. 5 Sep/Oct) 1997, pp. 84-93.}

[viii] Lawrence, P. and Lorsch, J. (1967), "Differentiation and Integration in Complex Organizations." *Administrative Science Quarterly,* Vol. 12 (1), June 1967, pp. 1-47;
Lawrence, P. and Lorsch, J. 1967. *Organizations and Environments: Managing Differentiation and Integration*. Harvard Business School Press, Cambridge, MA;
Lawrence P. and Lorsch, J. 1969. Organization-Environment Interface. In *Developing Organizations: Diagnosis and Action*. Reading, Mass: Addison-Wesley Publishing, 23-30.

[ix] M. Iansiti and J. West, "Technology Integration", *Harvard Business Review*, May-June 1997, pp. 69-79; -- M. Iansiti, *Technology Integration: Making Critical Choices in a Dynamic World*, Harvard Business School Press, Cambridge, Mass, 1998.

[x] Integration of industrial parameters through multiplicative models is described in Jay W. Forrester, *Industrial Dynamics*, Cambridge, Mass.: Productivity Press (1961).

[xi] Some of these methods are described in D. G. Ancona and D. F. Caldwell, "Bridging the Boundary: External Activity and Performance in Organizational Teams," *Administrative Science Quarterly,* 37: (1992), pp. 624-635.

[xii] Technology integration knowledge is very "sticky": it is difficult to generate, acquire or transfer {E. von Hippel, "'Sticky Information' and the Locus of Problem Solving: Implications for Innovation," *Management Science* 40, No. 4, April 1994, pp. 429-439}, because it tends to be primarily tacit {Polanyi, M. (1966), *The Tacit Dimension*. Anchor Day Books, New York}. Knowledge transfer, in particular, is neither costless {D. Teece, Technology transfer by multinational firms: The resource cost of transferring technological know-how," *Economic J*., 87, 346, June 1977, pp.242-261} nor problem fee {Szulanski G. 1996 Exploring internal stickiness: impediments to the transfer of best practice within the firm. *Strategic Management Journal.* 17:27-43}. Knowledge is especially difficult to transfer in high velocity environments because time pressure increases the stickiness of information {C. Weber, "Knowledge Transfer and the Limits to Profitability: An Empirical Study of Problem-Solving Practices in the Semiconductor Industry," *IEEE Transactions of Semiconductor Manufacturing,* Vol. 15(4) Nov. 2002. pp. 420-426}. Study #1 demonstrates that integration knowledge, which cannot be transferred under time pressure, almost exclusively resides in integrating devices. Technology-specific knowledge, which can also not be transferred under time pressure, primarily resides in technology-specific subsystems. A two-step process for problem diagnosis has been observed in 31 out of 42 cases for which problem localization was not trivial. In the first step, the integrating device localizes the problem to a particular process technology. Technology specialists from the appropriate technology subsystem subsequently identify the root cause of the problem. An

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investment in automatic localization technology circumvents the integrating device in 10 out of 42 cases, and localization could be inferred from previous experience in one case. The value of problem localization can be quantified as the amount of information extracted per unit time {C. Weber, V. Sankaran, K. Tobin, and G. Scher, "Quantifying the value of ownership of yield analysis technologies," *IEEE Transactions of Semiconductor Manufacturing*, Vol. 15(4) Nov. 2002, pp. 411-419.}.

[xiii] The model was driven into theoretical saturation in a series of interviews that solicited the expertise of 61 specialists in a variety of disciplines that pertain to semiconductor manufacturing.

[xiv] For a description of the Pareto Principle please see Juran, J.M., Editor, *Quality Control Handbook* Third Edition, McGraw-Hill Book Company, 1974, pp. 2-16 to 2-19.

[xv] For a characterization of the relationship between batch yield and batch fault density and susceptibility to faults, which are known as *yield models* in semiconductor manufacturing, see, for example, C. Stapper, “Modeling of integrated circuit defect sensitivities,” *IBM J. Res. Develop.*, vol. 27, pp. 549-557, Nov. 1983; -- A.V. Ferris-Prabhu, "Modeling of Critical Area in Yield Forecasts", *Journal of Solid-State Circuits*, SC-20(4), pp. 878-880; -- or J. Cunningham, “The use and evaluation of yield models in integrated circuit manufacturing,” *IEEE Trans. Semicond. Manufact.*, Vol. 3, no. 2, pp. 60-71, May 1990.

[xvi] Justus von Liebig (1803-1873) was a German chemist who spent the early part of his accomplished career as a pioneer in organic chemistry. He turned to what is now called biochemistry in about 1838, and first published on agricultural chemistry in 1840. He made numerous significant advances and engaged in extensive, fruitful debate with other researchers in the field. Liebig argued that crop yield is the multiplicative product of factors such as concentration of nitrates, phosphates and sunlight. Crop yield is limited by the most deficient factor. Adding extra phosphates will not increase crop yields, if the soil is deficient in nitrates. {Wallace, A. & G. A. Wallace, “Limiting factors, high yields, and law of the maximum.” *Horticultural Review*. New York, NY: John Wiley & Sons, Inc. Press. 1993. v. 15, p. 409-448.}

[xvii] Historically, learning by doing {K. Arrow, “The Economic Implications of Learning by Doing,” *Review of Economic Studies* 29 (1962): pp. 155-173} and the learning curve {e.g. Argote, L., and D. Epple, "Learning curves in manufacturing," *Science*, Vol. 247 (1990), pp. 920-924} have been viewed primarily from the point of view of cost reduction. Study #3 of this dissertation stresses the importance of learning how to increase revenue.

[xviii] In semiconductor manufacturing, the timing of market windows can frequently be predicted from Moore’s Law {Moore, G. (1975), “Progress in digital integrated circuits,” *IEDM Tech. Dig.*, p. 11.} Semiconductor manufacturers can generally estimate the timing of their market windows a few years in advance, and plan their product and process development strategies accordingly.

[xix] e.g. Hannan, Michael and John Freeman. 1989. *Organizational Ecology*. Cambridge: Harvard University Press; -- Freeman, John and Warren Boeker. 1984. The ecological analysis of business strategy. *California Management Review*, 26: 73-86.

[xx] Companies that are in a dominant market position possess the ability to strategically orchestrate, encourage and coordinate complementary innovation, and these activities can create additional demand for their products that could ameliorate unit price erosion. For example, Intel Corporation influences the direction and pace of development of other products by a large number of third parties in the computer industry. {Gawer, A. and M. Cusumano, *Platform Leadership: How Intel, Microsoft and Cisco Drive Industry Innovation*, Cambridge, Mass.: Harvard Business School Press, May 2002.}

[xxi] Walt Trybula, Presentation of International SEMATECH's Global Economic Model [for semiconductor manufacturing], Portland, Oregon, May 20th, 2003.

[xxii] In the tradition of Peirce, Charles Saunders (1898/1992), *Reasoning and the Logic of Things*, Harvard University Press: Cambridge, MA; -- and James, William (1907), *Pragmatism*, The American Library: New York, NY.

[xxiii] Learning-by-doing occurs through 'interference finding' {E. von Hippel and M. Tyre, "How leaning by doing is done: problem identification in novel process equipment," *Research Policy* 24 (1995) pp. 1-12}, a process of discovering anomalies through procedures that resemble imaging techniques. Recent evidence from the semiconductor technical literature suggests that interference finding is being automated {e.g. M. H. Bennett, K. W. Tobin, and S. S. Gleason, "Automatic Defect Classification: Status and Industry Trends," *SPIE Metrology, Inspection, and Process Control for Microlithography IX*, Vol. 2439, p. 210, San Jose, CA, March 1995; -- Gary Scher, Dennis Eaton, James Sorensen, Barry Fernelius and Jerry Akers, "In-line statistical process control and feedback for VLSI integrated circuit manufacturing," *IEEE Transactions on Components, Hybrids and Manufacturing Technology*, Vol. 13, No. 3, pp. 484-489, September 1990; -- K. W. Tobin, S. S. Gleason, T. P. Karnowski, S. L. Cohen, and F. Lakhani, "Automatic Classification of Spatial Signatures on Semiconductor Wafermaps", *SPIE 22nd Annual International Symposium on Microlithography*, Santa Clara, California, March 9-14, 1997} In addition, the ability to solve problems jointly and simultaneously across distances becomes source of competitive advantage in high velocity environments {C. Weber, "Knowledge Transfer and the Limits to Profitability: An Empirical Study of Problem-Solving Practices in the Semiconductor Industry," *IEEE Transactions of Semiconductor Manufacturing,* Vol. 15(4) Nov. 2002. pp. 420-426}. All of these techniques tend to "unstick" knowledge rapidly, enhancing its transferability in high velocity environments. [xii] Organizations become less rigid and thus more resilient to environmental shifts. [xix]

[xxiv] For a description of the nature and economics of the Yield Ramp please see Terwiesch, C., and R. E. Bohn (2001), "Learning and Process Improvement During Production Ramp-Up," *International Journal of Production Economics* 70(1): 1-19.

[xxv] Normalized performance factors can be viewed as yields, and yield improvement can be viewed as waste reduction. Approaches to waste reduction have been described from a theoretical perspective {P. B. Kantor & W. I. Zangwil, "Theoretical Foundation for a learning rate budget," *Management Science*, Vol. 37, No. 3, pp. 315-330.}, in relation to organizational learning in quality projects {M. A. Lapré, A. S. Mukherjee & L. N. Van Wassenhove, "Behind the learning curve: linking learning activities to waste reduction," Working paper 96/34/TM, INSEAD;-- A. S. Mukherjee, M. A. Lapré & L. N. Van Wassenhove, "Knowledge-driven quality improvement," *Management Science*, 44 (11) (1998), pp. 35-44.}, as well as in relation to knowledge creation and knowledge transfer {M. A. Lapré, & L. N. Van Wassenhove (2001), "Creating and transferring knowledge for productivity improvement in factories," *Management Science*, Vol. 47, No. 10, October 2001, pp. 1311-1325}.

[xxvi] Cost of Ownership (CoO) models strongly influence financing decisions, purchasing decisions and manufacturing practices in the semiconductor industry. For a description of the line of reasoning behind CoO models please see R. Carnes and M. Su, "Long term Cost of Ownership," *IEEE/SEMI Int'l Manuf. Sci. Symp.* 1991, pp. 39-43; R. Martinez, V. Czitrom, N. Pierce and S. Srodes, "A methodology for optimizing Cost of Ownership," *SPIE* Vol. 1803 (1992) pp. 363-387; J. Secrest and P. Burggraaf, "The reasoning behind Cost of Ownership," *Semiconductor International*, May 1993; R. Doering, "Cost-of-Ownership issues in a flexible manufacturing environment," *Solid State Technology*, Feb. 1994, pp. 39-43; D. Dance and D. Jimenez, "Applications of Cost of Ownership," *Semiconductor International*, Sept.1994, pp. 6-7.

[xxvii] "It is widely agreed upon among students of corporate finance that, for practical purposes, the most appropriate evaluation criterion for a corporate investment project is the net present value (NPV) of the project." {U. Reinhardt, "Breakeven analysis of Lockheed's Tristar: An application to financial theory," *Journal of Finance* 28 (4), Sept. 1973, p. 822.} Net present value covers cost and revenue of learning phenomena, as well as the discount rate.

[xxviii] A modern semiconductor process consists of about 500 process steps and a total of about 2000 parameters, each of which evaluates a unique learning experience to which statistical quality control procedures {e.g. Deming, W. E. (1982), *Quality, Productivity and Competitive Position*, MIT Center for Advanced Study, Cambridge, MA.} can be applied. The learning architecture in figure 10 allows managers to assess contribution how each of these parameters contributes to the financial bottom line. In figure 10, NPV(t) represents the performance of the organization as a whole.[xxvii] NPV(t) is broken down into a revenue component – the revenue generation rate R(t) – and a cost component – the total cash outlay rate C(t). The discount rate or opportunity cost of capital $\kappa(t)$ becomes an important parameter because industrial lifecycles last over many years. R(t) is given as the multiplicative product of unit price P(t) of the product under production and the maximum product output rate Q(t). C(t) is determined by cost of ownership models.[xxvi] The susceptibility to faults S(t), product unit price and a calculable portion of cost outlays associated with product design $C_{des}(t)$ are product specific, and can be associated with the product design subsystem. Cost of ownership, process-engineering metrics $\{F_{batch}(t)\}$ and production metrics (line yield $\{Y_{line}(t)\}$, maximum batch throughput rate $\{T_{prod}(t)\}$ can be broken down by process technology (j) and ultimately to the individual process step (k).