Learning Leverage under Time-to-Market Pressure: A Key Success Factor in High Technology Manufacturing[1]

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Abstract *– An empirically grounded model of the lifecycle of a microprocessor-manufacturing venture extends organizational learning theory to cover the high technology manufacturing environment. The model presents evidence that organizational learning can be leveraged to cope with time-to-market pressure. Prolonged, sustained investments in learning at a relatively constant level generate highly non-linear surges in financial performance, but financial performance deteriorates as market windows draw to a close. Analysis of the model indicates that a slight, but coordinated acceleration of the organizational learning rate enhances profitability more than any other factor does. Factors such as maximizing product quality, increasing scale or reducing a product's susceptibility to quality problems are subordinate and reach diminishing returns. A select few firms, which are in a position to exercise* platform leadership *(Gawer & Cusumano, 2002), can increase a microprocessor manufacturing venture's profitability by delaying product price erosion. The theory developed in this paper can, in principle, be extended to other industries within or outside the high technology environment.*

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1. INTRODUCTION

Organizational learning theory has successfully characterized industrial activities in which unit labor cost or unit cost of production decreases at a decreasing rate as organizations produce more of a product (e.g. Argote & Epple, 1990). This phenomenon, which is attributed to increasing skill in production, is generally referred to as the learning curve, the experience curve, the progress curve or 'learning by doing'. Organizational learning theory has been expanded to cover the observed variability in learning rates (e.g. Dutton & Thomas, 1984), which can be attributed to phenomena such as ‘organizational forgetting’ (Argote, Beckman & Epple, 1991) or knowledge transfer (e.g. Hatch & Mowery, 1998); the consequences of learning at different levels of cognitive complexity (Hirsch, 1956; Fellner, 1969; Dudley, 1972; Adler & Clark, 1991); some of the inner mechanisms of learning by doing (Adler & Clark, 1991; von Hippel & Tyre, 1995); as well as the acquisition of production skills prior to the release of a product (Pisano, 1996). However, to date, organizational learning theory does not comprehensively characterize learning in high technology manufacturing industries, which tend to be yield driven (Bohn & Terwiesch, 1999) and constrained by finite market windows (Eisenhardt, 1989b). In combination, these attributes of the high technology manufacturing environment subject high technology manufacturing firms to *time-to-market pressure*: for a high tech manufacturing venture to be profitable, it needs to be completed within a particular timeframe.

In this paper, I investigate organizational learning under time-to-market pressure in a high technology manufacturing setting. I propose a theoretical framework that allows high technology manufacturing firms to respond to the time-to-market challenge through *leveraged learning* efforts, which take advantage of non-linear relationships between investments in learning and the performance rewards that these investments can provide. I address the specific research question, "Which investments in learning offer the highest *learning leverage* in a high technology manufacturing venture?" As candidates for learning levers I nominate investments in *quality learning*, which reduces the number product-disabling faults observed in products that emerge from the manufacturing line; *volume learning*, which allows one or multiple factories to ramp up or increase scale rapidly; and *design learning*, which may enhance quality learning by reducing a design's susceptibility to faults, i.e. making the design more 'robust'. All three forms of learning can proceed concurrently and independently, and each may have a different impact on the profitability of a high technology manufacturing venture, which I respectively term *quality leverage*, *volume leverage* and *design leverage*.

In this paper, I present evidence all three of the aforementioned high technology learning levers are subordinate to *time leverage*, which I define as the impact on profitability of slightly accelerating quality learning, volume learning or design learning. I shall show that time leverage increases the financial performance of high tech manufacturing ventures exponentially, whereas the other levers all yield diminishing returns. Time leverage is especially powerful when an organization makes a coordinated effort to accelerate quality learning and volume learning. In general, time leverage is exercised by improving problem-solving practices associated with quality-, volume- and design learning. However, the results of the study imply that a select few firms, which are in a position to exercise *platform leadership* (Gawer & Cusumano, 2002), can leverage time by stimulating demand for the product to be manufactured, a course of action that extends the product's market window or delays product price erosion.

The above theoretical framework is tested in an empirical study of semiconductor process development and microprocessor manufacturing practices. The results of the empirical study are expressed in terms of a numerical model that quantifies the profitability of microprocessor manufacturing throughout a complete semiconductor process lifecycle. Microprocessor manufacturing has been chosen as a setting for this study because it is characterized by time-to-market pressure that results from a continuous, relatively non-volatile erosion of product unit prices,[i] and by a highly non-linear relationship between the investment in learning and the resulting performance. Microprocessor manufacturers also fit Terwiesch & Bohn's (2001, p. 5) definition of high technology manufacturing firms, as companies that are "on the cutting edge of what is currently understood in process engineering."

The remainder of this paper is organized as follows. Section 2 provides a theoretical framework for leveraged learning in a high technology environment, which is grounded in the management literature. Section 3 discusses the research methods upon which the empirical study in this paper is based. Section 4 describes the Microprocessor Profitability Model, which articulates the results of the empirical study. In section 5, key variables of the Microprocessor Profitability Model are varied, *ceteris paribus*, to determine which among them possesses the highest leverage with respect a high technology venture's profitability. Section 6 implies that the results of the study can be generalized beyond microprocessor manufacturing and high technology industries. It also suggests topics for further research.

2. LEARNING IN HIGH TECHNOLOGY INDUSTRIES

Studies of a variety of industrial activities, including airframe construction (Wright, 1936, Alchian, 1963), manufacturing machine tools (Hirsch, 1952), refining petroleum products (Hirschmann 1964), the production of ships (Rapping 1965) and the construction of power plants (Zimmerman 1982; Joskow & Rose 1985), have shown that the unit cost of production decreases at a decreasing rate as produce more of a product (Argote & Epple, 1990). This phenomenon is generally referred to as the learning curve, the experience curve, the progress curve or 'learning by doing' (terms that shall henceforth be used interchangeably despite subtle differences in definition[ii]). It is attributed to increasing skill in production, and its characterization is based on the following assumptions.

1. Cumulative output is a valid proxy for learning. Simply producing more units constitutes an investment in learning.
2. The rewards for learning are essentially instantaneous. Unit costs drop as organizations learn.
3. The unit cost of production characterizes the performance that results from organizational learning. Learning does not affect revenue generation.

None of these assumptions appear to be consistent with a significant number of studies that have been conducted in high technology environments. For example, Adler & Clark (1991) challenge the notion that learning is primarily a function of cumulative output. In their study of an anonymous high technology firm, they differentiate between learning of the first and second order. The first order includes direct informal, behavioral, tacit, single-loop (Argyris & Schon, 1978), autonomous forms of learning, which are captured by the traditional experience variables that are associated with the learning curve. The second order covers more formal, cognitive, explicit, double-loop (Argyris & Schon, 1978), induced forms of learning, which transforms the goals of the process by explicit managerial and engineering action. Specifically, engineering changes and formal training programs can affect the technology, the equipment, the processes or human capital in ways that augment capabilities. Adler and Clark introduce what they call "managerial variables" such as Cumulative Engineering Activity (CENG) and Cumulative Training Activity (CTRN) to measure the investment in second order learning. CENG tracks the cumulative number of hours spent by direct personnel in activities associated with product design changes either running new experiments or learning new specifications. CTRN accounts for the number of hours that direct personnel expends in on-the-job training, which is principally conducted by coworkers doubling up on a work post.

In his study of the pharmaceutical industry, Pisano (1996) observed that much of the learning contributing to the reduction of unit cost can take place before a new product or process design is introduced into the factory. This phenomenon, which Pisano (1996) calls ‘learning before doing’, occurs through computer simulations, laboratory experiments, prototype testing pilot production runs and other experiments. Its intent is to facilitate a seamless transition between research, development and production: if many quality and production issues are settled before product introduction the ramp to production can be viewed as an increase in scale. In Pisano’s (1996) study, learning before doing primarily occurs in environments such as chemical synthesis, where underlying industrial knowledge is deep. By contrast, industries like biotechnology, where underlying theoretical and practical knowledge is relatively thin, rely on learning by doing for efficient development.

Pisano’s (1996) observation of learning before doing in the pharmaceutical industry violates two assumptions of the learning curve. Firstly, organizational learning is not simply a function of cumulative product output because it can occur before there is any product output. Secondly, the reward in performance that is associated with organizational learning is not necessarily instantaneous. For example, a pharmaceutical firm may acquire production skills years before it puts them to use on sellable product. By the time the firm has released sellable product, ramped up to volume production and is generating significant revenues, most of its organizational learning may already have been done: the firm may be reaping the performance benefits of prior investments in learning. Even though its cumulative output is rising dramatically during volume production, the firm may be learning next to nothing new.

The conclusions derived from Pisano's (1996) observations are consistent with the results of studies that have been conducted in yield-driven industries such as disc drive fabrication (Bohn & Terwiesch, 1999) and various types of semiconductor manufacturing (Bohn & Terwiesch, 1999; Terwiesch & Bohn, 2001). Both of these industries rely on batch processing, and exhibit a highly non-linear relationship between quality and batch yield, a variable that Bohn (1995) defines as the fraction of units of product within a batch that can be sold. A prolonged, sustained, constant effort in quality improvement reaps a delayed non-linear performance reward, which manifests itself in the form of a surge in batch yield. In effect, yield-driven industries exhibit quality leverage: unit cost of production remains at very high values throughout most of the quality learning effort, but it drops dramatically as batch yield surges (Weber, 1996).

If the unit price of the produced good remains constant, then the timing of a surge in batch yield has a minor influence on profitability. The benefits of learning manifest themselves in cost reduction, exclusively. However, firms in high technology industries frequently operate in what Eisenhardt (1989b) calls "high velocity environments", where "making the market window" can be the primary determinant of success or failure. In high velocity environments, the unit price of the good to be sold may fluctuate. Unit price may, for example, exceed unit cost of production by and order of magnitude in the early stages of production, but erode continuously until the revenue generation rate permanently drops below the cost outlay rate, i.e. the market window closes forever. Under these circumstances, the impact of learning is clearly time dependent, and the benefits of leveraged learning manifest themselves in additional revenue. To maximize profit, the high technology firm must learn to produce at high volumes while unit price is high. Cost reduction becomes a major factor once unit price has eroded to the point where it no longer significantly exceeds unit cost.

An in depth look into learning in high technology environments suggests that practicing managers, engineers and workers in high technology industries use neither cost nor revenue as performance metrics for their learning activities. For instance, benchmarking studies (Leachman, 1996; Leachman & Hodges, 1996) and longitudinal studies (e.g. Stapper & Rosner, 1995; Weber, Moslehi & Dutta, 1995) of semiconductor manufacturing and process development indicate that semiconductor manufacturers use batch fault density (the number of faults within a batch that have ruined a product) as their primary performance metric for quality learning and factory throughput (the number of batches that exit the factory per unit time) as their primary performance metric for volume learning. The impact of batch fault density and factory throughput on financial performance is not mentioned in any of these studies, in part for reasons of confidentiality, but also because the link between these types of learning and profitability is not completely understood.

The above studies of the semiconductor R&D and production environment display their performance data as a function of calendar time, a meaningful approach if semiconductor-manufacturing organizations sustain a continuous learning effort at a constant level. Using calendar time as a proxy for the investment in learning is also consistent with a significant number of studies, which have investigated phenomena that encompass complex cognitive processes in environments other than high technology. For example, Hirsch (1956) was one of the first to notice that the rate of change in labor productivity rose with production experience. In addition to a simple learning process that explains productivity changes on a single job, Hirsch postulated the existence of a separate learning-to-learn process to explain an increase in the progress ratio between jobs. Fellner's (1969) study of Olympic sports identified an analogous phenomenon. The study concluded that performance was closely related to cumulative output in simpler sports, where there had been few changes in equipment or rules. In sports where rules or equipment had changed, or in sports that were characterized by more complex strategies, performance was better explained as a function of time.[iii]

The findings of the above studies suggest that an expansion of organizational learning theory, which covers learning in the high technology environment, should exhibit the following attributes. Firstly, both the performance metric and the proxy for the learning investment must acknowledge the fact that a large portion of the learning that takes place in a high technology venture occurs before the start of production (Pisano, 1996). Secondly, learning in high technology industries is likely to involve complex cognitive processes such as learning how to learn (Hirsch, 1956; Fellner, 1969; Dudley, 1972). Time should thus serve as a proxy for the learning investment. Thirdly, employing activity-specific performance metrics such as batch fault density and factory throughput, which practitioners in high technology manufacturing ventures utilize to evaluate actual industrial learning efforts, provides insight into how and when learning occurs. Fourthly, learning that occurs in high velocity environments (Eisenhardt, 1989b) or under time-to-market pressure is likely to be time sensitive. A skill that is critical for revenue generation is likely to be more valuable in times when product unit price is high than when it is low. Thus the global financial performance metrics that characterize learning in high velocity environments or under time-to-market pressure must be sensitive to both time and revenue generation. Finally, the learning activities and their specific impact on the bottom line must be integrated into the expression global financial performance.

Net Present Value (NPV) satisfies all of the above criteria for acting as a global performance metric for high technology ventures. NPV can be used to describe performance prior to product release, it is sensitive to time, and it contains a term that describes the revenue of a venture. In addition, Net Present Value is sensitive to the discount rate associated with a venture, a highly useful attribute for a parameter that characterizes the performance of high technology ventures whose lifecycles may span a decade, a period of time that is long enough for the time value of money to matter. Therefore, "it is widely agreed upon among students of corporate finance that, for practical purposes, the most appropriate evaluation criterion for a corporate investment project is the Net Present Value of the project (Reinhardt, 1973, p. 822)," a high tech investment project being no exception.

In summary, a theory of learning that covers the high technology environment can be expressed as a mathematical model, in which calendar time acts as the proxy for the learning investment, practical performance metrics characterize the various types of learning that occur in a high tech organization, Net Present Value serves as a global financial performance metric, and functional relationships describe the leverage that learning efforts exert on a high technology venture's financial performance. All coefficients in the mathematical model need to be determined empirically.

3. METHODOLOGY

This paper builds and tests a theory for organizational learning for ventures that operate in high technology environments by conducting an empirical study of semiconductor process development and microprocessor manufacturing practices, whose results are expressed in terms of a mathematical model. The empirical portion of this paper relies upon the method of extended case study research, which is described in Yin (1981) and Eisenhardt (1989a). Data for the study in this paper come from multiple sources, including published semiconductor benchmarking studies (Leachman, 1996; Leachman & Hodges, 1996); historical performance data of individual companies (Stapper & Rosner, 1995; Weber, Moslehi & Dutta, 1995); projections of technical trends, which are published in the Semiconductor Industry Association's 2001 edition of the International Technology Roadmap for Semiconductors (SIA-ITRS)[iv]; and 69 case interviews with 37 respondents. Data are transcribed, coded, analyzed and converted into a numerical "Microprocessor Profitability Model", which characterizes a semiconductor process lifecycle of the kind that microprocessor manufacturers are likely to experience. An additional series of interviews that solicit the expertise of 61 specialists in a variety of disciplines that pertain to semiconductor manufacturing is conducted to drive the Microprocessor Profitability Model into theoretical saturation. Experts are recruited by recommendations from within their respective peer groups.

Additional details regarding data collection, and analysis are given in Appendix A.

4. THE MICROPROCESSOR PROFITABILITY MODEL

The Microprocessor Profitability Model uses the data from the empirical study in this paper to create a realistic picture of the lifecycle of a semiconductor manufacturing process and the environment in which microprocessor manufacturers operate. The Microprocessor Profitability Model consists of two parts: a manufacturing model and a financial model. The manufacturing model determines the total manufacturing rate – the number of products that a venture can manufacture per unit time – from factors such as batch size, batch quality and batch output rate, which can all be influenced by a sustained learning effort. The financial model ascertains the expected profitability of a semiconductor venture from the output of the manufacturing model and key financial variables such as opportunity cost of capital and product unit price. The output of the financial model is expressed in terms of Net Present Value, which like many of the factors that determine the success of a semiconductor venture, can vary significantly over time.

The Microprocessor Profitability Model assumes that success of a microprocessor-manufacturing venture to a great degree depends upon learning how to execute tasks that involve complex operations, an ability that Fellner (1969) and Dudley (1972) believe to be time dependent. Thus the time that has elapsed since the inception of the venture 't', acts as the independent learning variable that represents the learning investment. The time since venture inception is set to zero at the commencement of learning activities. This event is assumed to occur when a firm that intends to manufacture particular microprocessor product starts to simulate the characteristics of the product, to model the microelectronic devices and semiconductor processes by which the product will be realized, or to begin the first experiments that pertain to this process (Thomke, 1998), whichever transpires first.

4.1 The Manufacturing Model

Semiconductor manufacturing in general and microprocessor manufacturing in particular relies on batch processing. Silicon wafers act as batches for products, which are known as integrated circuits (ICs), "chips" or "dice". The manufacturing line consists of a series of fabrication, metrology and inspection steps, which are executed on process, metrology and inspection equipment, respectively; there are no assembly steps in the line. Integrated circuits can be destroyed by contaminants with volumes smaller than one thousandth of a cubic micrometer. Thus process, metrology and inspection equipment reside inside a clean room fabrication facility called a "fab". Chips are tested for functionality and electrical characteristics at the end of the manufacturing line, when they are still part of a silicon wafer but can be safely removed from the fab. Product failure occurs when these tests detect an anomalous electrical signal called a "fault", which precludes an integrated circuit product from being sold.

4.1.1 Quality Learning, Design Learning and Volume Learning

The manufacturing model derives the total manufacturing rate from the three learning phenomena that can practitioners can observe and quantify in microprocessor manufacturing: quality learning, design learning and volume learning. Quality in microprocessor manufacturing is given in terms of the batch fault density ($F_{batch}(t)$), which is defined as the number of faults detected per batch at a particular time since venture inception (t). A product-design-specific parameter called the critical area (A(t)), quantifies the susceptibility to faults of a particular product at a particular time since venture inception (t). The critical area is defined as the surface area chip that is susceptible to faults. Since integrated circuits are viewed as planar entities, critical area is given in square centimeters, and batch fault density is given in faults per square centimeter of critical area.[v] A reduction in fault density over a period of time is considered evidence for performance that is derived from quality learning. A reduction in critical area, which occurs from design revision to design revision, is considered as evidence of performance that results from design learning: it implies that designers have made a product more "robust" by reducing its susceptibility to faults.

Practitioners in the semiconductor industry quantify a semiconductor fab's production performance in terms 'wafer outs', a colloquialism for the wafer (batch) output rate (W(t)) – the number of wafers (batches) per unit time that emerge from the fab intact at a particular time since venture inception (t). An increase in the wafer output rate over time is considered as evidence of performance improvement that results from volume learning: contrary to the findings of Hirsch's (1952) seminal study on machine tools, which concluded that learning and scale are separate phenomena, most of the respondents in this study that possess extensive semiconductor manufacturing experience believe that the ability to ramp from R&D to production levels in a short time needs to be learned. In the words of an expert in semiconductor diagnostics:

> *"You cannot just crank up a wafer fab like the volume knob on your stereo. It requires some learning. You will add more equipment. You may have to add and manage additional shifts in maintenance and production. Equipment problems that do not occur when you run at low volume are likely to appear. For example, robotic loading equipment is more likely to fail if you run it perpetually without maintenance. … You may also have to remove a few unnecessary [diagnostic] steps from the process to minimize your WIP [work-in-progress] inventory. You will have to learn how to run the fab without the information that these [diagnostic] steps reveal."*

4.1.2 Quality Leverage, Design Leverage and Volume Leverage

The outcome of the empirical study in this paper, upon which the Microprocessor Profitability Model is based, suggests that quality learning, design learning and volume learning are leveraged, and that learning leverage in microprocessor manufacturing can be derived from three factors. Firstly, problem-solving practices for all three forms of learning proceed according to the Pareto Principle (Juran, 1974, 2-16 to 2-19). Problem solvers choose the solution alternative that they believe will close the largest portion of their perceived gap between desired and actual levels of performance (Newell & Simon, 1972; Iansiti & Clark, 1994; Pisano, 1996). If the performance gap results from multiple problems, and the resources for solving them all in parallel are unavailable, then the problem solvers will attack the worst problems – the ones whose solution they believe will close the largest portion of the performance gap – first, and proceed in decreasing order of problem severity. In the words of a 20-year veteran of semiconductor manufacturing and process development,

> *"Solving problems in semiconductor process development is like peeling an onion. You remove the largest layer first, and you will find another [somewhat smaller] layer underneath."*

Volume leverage is achieved through a constant, sustained problem-solving effort that focuses on increasing the wafer output rate W(t). Problems are solved in decreasing order of the perceived impact on wafer output rate which ultimately results in an exponential surge in W(t). A manager at a firm, which provides yield management consulting services to many microprocessor manufacturers, explains how this occurs.

> *"From what I observe at our customers, the initial ramp to volume is very painful, but gets a lot easier as time progresses. … You are removing bottlenecks at every process step in the line. You remove the worst bottlenecks first. In the beginning, there are many bottlenecks, so your efforts do not make much difference. Once there are few bottlenecks left, your efforts begin to pay off. Your throughput rises dramatically."*

Process engineers in fabs generate *quality leverage* by solving quality problems in decreasing order of perceived impact on batch fault density, but fault density decays exponentially in response. Analogously, design engineers induce *design leverage* by making design changes in decreasing order of their perceived impact on critical area, which decreases at a decreasing rate from design revision to design revision.

The yield-driven nature of microprocessor manufacturing provides additional leverage for quality learning and design learning (Bohn & Terwiesch, 1999). The batch yield of a particular product at a particular time (t) can be expressed as

$$Y(t) = e^{-A(t) * F_{batch}(t)} \qquad (1),$$

where 'e' denotes the natural logarithmic constant (~2.718).[vi] Equation (1) suggests that batch yield[vii] can be increased exponentially over time either by a linear reduction in batch fault density or a linear reduction in critical area. However, due to Pareto-driven quality learning and design learning, batch fault density and critical area decay exponentially as a function of time, making batch yield extremely sensitive to time since venture inception.

4.1.3 Coordinated Learning Efforts

The total manufacturing rate of a factory that produces a particular product can be given as

$$Q(t) = Q_{batch}(t)\ Y(t)\ W(t) \qquad (2),$$

where $Q_{batch}(t)$ denotes the number of realizations of a particular product design that can be contained within a batch, or the number of chips of type that can be realized on one silicon wafer. Design learning can increase the number of products per batch over time since venture inception by shrinking the critical area of a chip from design revision to design revision. Substituting equation (1) into equation (2) yields equation (3), an expression for the total manufacturing rate, which is a highly non-linear function of (t).

$$Q(t) = Q_{batch}(t)\ e^{-A(t) * F_{batch}(t)}\ W(t) \qquad (3).$$

Equation (3) suggests that different learning efforts can be coordinated to maximize output. According to equation (3), a microprocessor manufacturer, who makes a constant, Pareto-driven effort at reducing batch fault density, initially experiences a prolonged period of time where batch yield remained near naught in spite of this effort. During this research and development (R&D) phase of the lifecycle of the semiconductor process that manufactures microprocessors, the total manufacturing rate will remain at a small fraction of its potential maximum regardless of the wafer output rate, suggesting that batch fault density drives the manufacturing rate when batch fault density is high. However, when batch fault density drops to levels where batch yield is significant, batch yield is likely to surge, giving the microprocessor manufacturer an incentive to concurrently ramp up to volume production (VP) and to improve process quality by reducing the fault density (Terwiesch & Bohn, 2001). This coordinated learning effort, known as the "Yield Ramp" in semiconductor manufacturing, increases the total manufacturing rate Q(t). However, once batch yield approaches unity, the incentive to reduce fault density disappears and quality leverage subsides. The microprocessor manufacturer can only increase the total manufacturing rate Q(t) of a particular product design by augmenting the wafer output rate W(t), or by reducing the critical area A(t) from design revision to design revision.

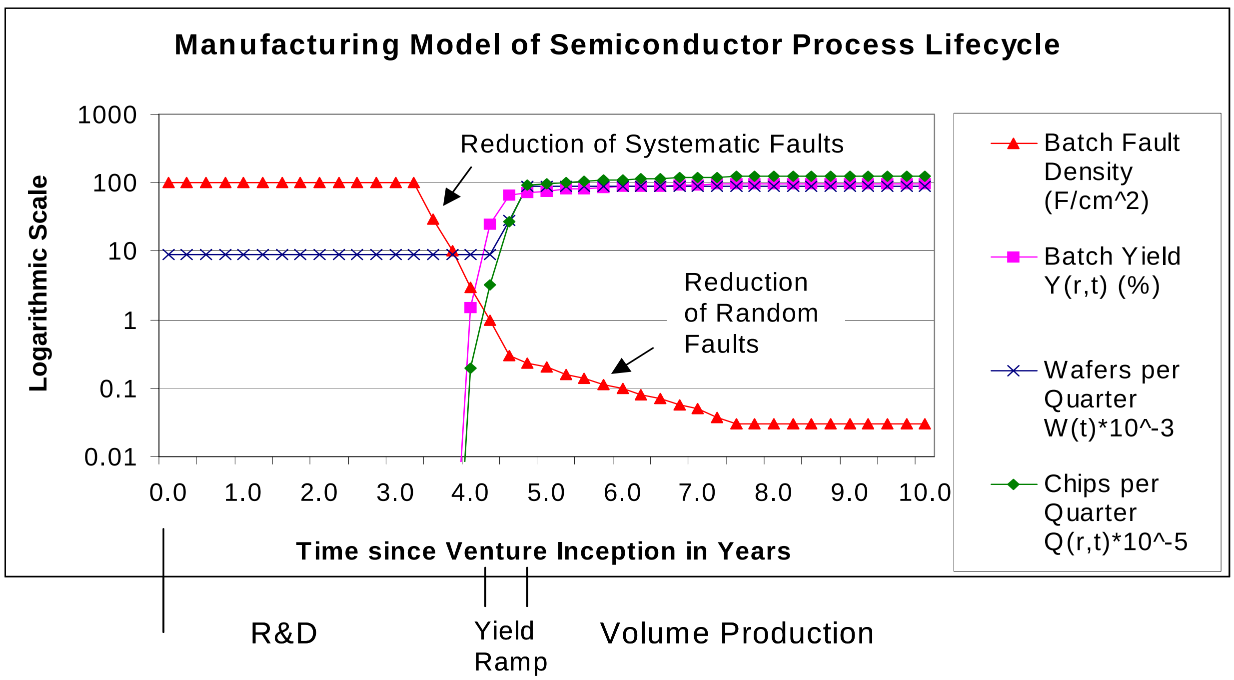

Figure 1: **Manufacturing model of the semiconductor process lifecycle that has been customized to the manufacture of a single microprocessor design. All values are plotted on a semi-logarithmic scale. The batch (wafer) output rate (W(t)) is given in thousands of wafers per quarter. The total manufacturing rate (Q(t)) is given in hundreds of thousands of chips per quarter.**

4.1.4 The Semiconductor Process Lifecycle for Manufacturing Microprocessors

Figure 1 illustrates the effect of coordinated learning on the lifecycle of a microprocessor manufacturing process. Figure 1 is derived from interviews with 29 experts in semiconductor technology integration and yield management, and semiconductor trend data from the 2001 edition of the SIA-ITRS. Figure 1 is based on a few assumptions, henceforth known as 'baseline conditions', which typify the experience of a manufacturer of microprocessors that is not the market leader. Two of these assumptions are physical: a time-invariant critical area A of 1.41 cm^2 and silicon wafers with a 200-mm diameter, which act as batches for 141 chips. Figure 1 illustrates the baseline assumptions that pertain to the evolution batch fault density and the consequences of coordinating fault reduction efforts with the time of the Yield Ramp. From this point on, the Microprocessor Manufacturing Model, will assume baseline conditions unless otherwise stated.

Figure 1 shows that, for more than the first three years of the semiconductor lifecycle, fault density can reside at levels above 100 faults per square centimeter, at which the batch yield of state-of-the-art microprocessors essentially equals naught. During this time period, the microprocessor manufacturer designs the flow of a semiconductor process by integrating its constituent technologies (Iansiti & West, 1997). The microprocessor manufacturer begins the fault reduction effort by performing extensive simulation of semiconductor process and device structures. The microprocessor manufacturer switches to physical experimentation once that learning mode eliminates more faults per unit time than simulation does (Thomke, 1998). These endeavors reduce fault density to a level at which batch yield is observable at significant levels[viii] on integrated circuit products. Batch fault density drops by orders of magnitude per year on an exponential trajectory as process-engineering teams correct systematic process failure mechanisms ("debug the process"). This effort ultimately leads to the surge in batch yield that is predicted by equation (3), triggering the Yield Ramp at time t_{ramp}, which under baseline conditions occurs about 4.25 years after venture inception. The rate of fault density reduction diminishes to a slower exponential trajectory once most process problems have been solved, and primarily randomly distributed faults, which tend to be caused by microscopic particulate matter known as micro-contaminants, remain. Process engineering teams remove micro-contaminants until batch yield approaches unity or the rewards of quality improvement reach diminishing returns (Terwiesch & Bohn, 2001).[ix]

The results of the empirical study, upon which the Microprocessor Profitability Model is based, suggest that the wafer output rate varies substantially across the semiconductor process lifecycle. (See Table 1.) For the first few years of a semiconductor venture a fab tends to run at an R&D level of about 100 wafers per day (~9000 wafers per quarter). This value is determined by an organization's need for experimentation capacity (Iansiti & West, 1997), which depends upon a plethora of factors such as process noise (Bohn, 1995), process complexity, and the throughput of the diagnostic tools in which a microprocessor manufacturer has invested. These factors vary from firm to firm and from fab to fab, causing the R&D output rate to vary substantially from venture to venture. The ultimate volume production level of the wafer output rate also varies from firm to firm. It depends upon economic factors such as the demand for the product (or portfolio of products) that the manufacturer produces and the costs production of manufacturing these products. According to the majority of the respondents, the volume production level exceeds the R&D output level by an order of magnitude. Thus the manufacturing model assumes a volume production level of 1000 wafers per day (~90,000 wafer per quarter). The wafer output rate rises from R&D levels to volume production levels during the Yield Ramp, which, according the respondents who have experienced or observed it, lasts between six months and one year. The manufacturing model assumes a six-month duration for the Yield Ramp, a value that is consistent with the performance of what the respondents call "best-of-breed" manufacturers, who have invested significantly in the ability to learn.

Table 1: Wafer Output Rate W(t) as a Function of Time since Venture Inception (t) for a Semiconductor Process Lifecycle (t_{ramp} denotes the start of the yield ramp.)

Lifecycle Phase *(y=years)*	*In wafers per day*	*In wafers per quarter*
R&D $(0 < t < t_{ramp})$	$W(t) = 100$	$W(t) = 9000$
YR $(t_{ramp} < t < t_{ramp}+0.5y)$	$W(t) = 100*10^{((t-t_{ramp})*2)}$	$W(t) = 9000*10^{((t-t_{ramp})*2)}$
VP $(t_{ramp}+0.5y < t)$	$W(t) = 1000$	$W(t) = 90{,}000$

Two factors limit the speed of the Yield Ramp to adding about 90,000 wafers per quarter every six months. Firstly, the installation of the additional units of process and diagnostic equipment that are required for volume production inherently takes a few weeks, and ramping up to full capacity in response to a batch yield signal cannot occur before said equipment installation is complete. A manager who was involved in installing large numbers of semiconductor process and diagnostic equipment has made the following comment.

> *"We brought the pilot facility up in near world record time, but the first wafers were out more than three months after we began installing the first pieces of equipment."*

The second limiting factor on the ramp rate is process noise (Bohn, 1995), which can obfuscate the statistical signals that are generated by a surge in Y(t) and an increase in W(t). A 25-year veteran of the semiconductor industry points out that measuring improvement during the Yield Ramp can be quite challenging.

> *"We always talk about yield ramping; we should be talking about the 'Yield Stair Steps'. In practice what happens is [batch] yield surges; the fab ramps up production. After a while, the fab has to interrupt the ramp to see whether the yield is still surging. You need to run under stable conditions for a while to see whether your process is still improving. True process control depends upon statistical significance.[x] … This [stop-and-go pattern] happens a few times during the Yield Ramp, and it takes time – weeks of time."*

4.2 The Financial Model

The financial component of the Microprocessor Profitability Model essentially consists of calculating the anticipated nominal cost outlays per unit time and the anticipated nominal revenues per unit time, whose difference reflects the anticipated nominal net profits per unit time. These nominal values are discounted at the expected opportunity cost of capital of the venture to reveal discounted cash flows per unit time. These discounted cash flows are subsequently summed up over the anticipated investment horizon to give an estimate of the expected cumulative revenues, expected cumulative costs and Net Present Value.

4.2.1 Nominal Cash Outlays – Operating Costs

The financial model calculates the nominal cash outlays of a semiconductor venture in terms of nominal "operating costs", which are a combination of the variable costs and the amortized fixed costs of the venture per unit time. Total Cost of Ownership (CoO) models, which have been customized for the semiconductor industry over the past 20 years, determine the operating costs from fixed costs and variable costs.[xi] CoO models translate the impact of the fixed costs of an asset into operating costs by distributing the fixed costs over the expected operating lifetime of the asset and adding that number to the variable costs. Nonetheless, operating costs vary over the semiconductor process lifecycle. The purchase price of semiconductor process and diagnostic equipment, which typically ranges from $1 million to $10 million per unit and has an expected lifetime ranging from three to six years before it becomes obsolete, can thus significantly affect the operating cost of a factory. These equipment-based operating costs persist whether or not the equipment is processing wafers. It is therefore in a microprocessor manufacturer's interest to develop a process on a core equipment set, which consists of the minimum number of units of equipment that are required to develop the process. This practice keeps operating costs associated with sustaining the equipment, i.e. labor, engineering, materials and consumables, to a minimum level, also. Once development efforts are successful, total batch fault density will have dropped to levels where the batch yield surges. The microprocessor manufacturer can anticipate conditions where batch yields are very high and, assuming demand exists for the integrated circuit that is to be produced, the venture will become profitable as soon as the factory can ramp up to volume production. At that point the factory may be producing under capacity constraint (Bohn & Terwiesch, 1999), giving the manufacturer a strong incentive to ramp up to volume production while batch yield is rising (Terwiesch & Bohn, 2001), i.e. proceed with the Yield Ramp. The microprocessor manufacturer purchases new equipment and hires additional personnel to maximize profits while producing under capacity constraint (Bohn & Terwiesch, 1999). Operating costs rise to a substantially higher level – one that reflects volume production conditions – and remain at that level throughout expected lifetime of the venture. If a venture exceeds its expected lifetime, then most of the fixed costs associated with the installed equipment have been amortized, i.e. the equipment has been paid off. Operating costs drop to a substantially lower level at that point in time. In summary, if we describe nominal cash outlays in terms of nominal operating costs, then the nominal cash outlays over the semiconductor process lifecycle can be approximated by a step function C(t), which is given in $ per unit time.

Table 2: Cash Outlay Rate (C(t)) as a Function of Time since Venture Inception (t) for a Semiconductor Process Lifecycle (t_{ramp} denotes the start of the yield ramp.)

Lifecycle Phase	***Cash Outlay Rate***
R&D ($0 < t < t_{ramp}$)	C(t) = $50 million per quarter
YR & VP ($t_{ramp} < t < t_{ramp}$+5 years)	C(t) = $150 million per quarter
Mature VP (t_{ramp}+5 years < t)	C(t) = $50 million per quarter

Cash outlays vary from company to company, but according to the majority of the respondents that are involved in semiconductor manufacturing and process development the values in Table 2 would be considered typical. During the R&D phase the manufacturer is likely to spend about $50 million in operating costs per quarter. This assumes amortizing $500 million in process equipment over a period of five years, sustaining an R&D organization of at least 500 technologists (product design, product development and process development) and consuming about 9,000 wafers per quarter. Shortly before the Yield Ramp the manufacturer has to more than double the personnel level, increase the wafer output by an order of magnitude and purchase about $ 1billion of plant equipment, which must be amortized during volume production. CoO models distribute these fixed costs over the expected lifetime of the process, which the financial model estimates to be five years beyond the start of the yield ramp. Under these conditions operating costs amount to about $150 million per quarter, an estimate that most respondents consider conservative for very large makers of microprocessors but in the ballpark for microprocessor manufacturers that are not market leaders. Quarterly operating expenses drop to about $50 million in mature volume production once equipment has been amortized and the manufacturer primarily pays for direct labor and materials costs. Within the R&D, volume production and mature volume production phases operating costs tend not to be volatile. The amortization of fixed costs proceeds at a predetermined rate that has been calculated by CoO models; the R&D organization does not grow or shrink significantly; and the materials costs do not fluctuate wildly.

4.2.2 Nominal Cash Revenues

The nominal cash revenue that is extracted from selling units of a product per unit time given by

$$R(t) = P(t)\, Q(t) \qquad (4),$$ [xii]

where the P(t) denotes the unit price of product at a time since venture inception (t), and Q(t) represents the sales rate, which equals the total manufacturing rate when a factory builds to order. The financial model assumes that the fab builds to order because microprocessor manufacturers, like most manufacturers, want to minimize inventories. Microprocessor manufacturers have an additional incentive to sell everything they can produce when they operate under capacity constraint, which can occur for a significant portion of their lifecycles (Bohn & Terwiesch, 1999). However, prices of microprocessors and many other integrated circuits[xiii] tend to decay exponentially over time, as production volume and the anticipated date for the release of substitute products nears. A manager who develops supply chain strategies for a maker of microprocessors explains.

> *"We have to get our products out as rapidly as possible, because our products have shelf life ... in a similar manner that vegetables in the supermarket have shelf life. … We may get half as much for a microprocessor a few months from now, and half as much again a few months after that. This presents a special problem for us. Our chips pass all specifications before we ship them, but unless we ship them fast we may not get a price that allows us to recover our costs. … The state of the art advances with Moore's law.[xiv] Unfortunately, so do the prices [They decrease as product performance of newer chips increases]."*

We may therefore approximate the unit price of an integrated circuit by the following expression.

$$P(t) = P(0)\, e^{-k_p t} \qquad (5),$$

where P(0) represents the price that a microprocessor manufacturer could get for a product at the inception of the venture, and k_p denotes the decay constant for price erosion. The financial model assumes conditions that are consistent with the evolution of microprocessor prices between 1995 and 2002. (Please see Appendix A.) These conditions can be approximated by setting P(0) to \$10,000 and k_p to 0.837, a value at which the nominal price drops by a factor of 10 every 2.75 years. Substituting equations (3) and (5) into equation (4) yields equations (6a) through (6c), which represent more detailed expressions for the nominal revenue generation rate.

$$R(t) = P(t)\, Q(t) = P(t)\, Q_{batch}(t)\, Y(t)\, W(t) \qquad (6a)$$

$$= \{P(r,0)\, e^{-k_p t}\} * \{Q_{batch}(t)\, e^{-A(t) * F_{batch}(t)}\, W(t)\} \qquad (6b)$$

$$= P(r,0)\, Q_{batch}(t)\, W(t)\, e^{-A(t) * F_{batch}(t) - k_p t} \qquad (6c).$$

4.2.3 Discounting and Net Present Value

The Microprocessor Profitability Model assumes that the lifecycle of a semiconductor manufacturing process extends for about a decade, from inception to obsolescence. This timeframe is sufficiently large for the time-value of money to become a significant factor in the financing of semiconductor ventures. As a result, the stream of cash revenues, cash outlays and net revenues need to be discounted at the effective annual cost-of-capital rate of the corporation that intends to undertake the semiconductor venture, which is given by the unitless constant κ. The continuously compounded discount rate (ρ) can be expressed in terms of (κ).

$$\rho = \log_e(1 + \kappa) \qquad (7)$$

The performance of the semiconductor venture is given in terms of Net Present Value, which acts as a general evaluation criterion for corporate investment projects (Reinhart, 1973, p. 887).

$$NPV(t,\kappa) = \int_0^\tau R(t)\, e^{-\rho t}\, dt - \int_0^\tau C(t)\, e^{-\rho t}\, dt \qquad (8),$$

where τ denotes the investment horizon, the last point in time for which a cash flow is posited. $NPV(t,\kappa)$ in equation (8) is a forward-looking metric. It estimates the total amount of profit that a venture expects to accrue by time $t=\tau$, and expresses this estimate in terms of dollar value at $t=0$, the venture's inception. The first term right hand side of equation (8) quantifies the revenues that have accrued between $t=0$ and $t=\tau$; the second term does likewise for the venture's cash outlays. In semiconductor manufacturing, $C(t)$ in equation (8) can be expressed as a step function such as the one that has been described in section 4.2.1, and equation (6c) can be substituted for $R(t)$ in equation (8).. Upon this substitution, cumulative revenue equals

$$\int_0^{\tau} R(t)\, e^{-\rho t}\, dt = P(r,0) \int_0^{\tau} Q_{batch}(t)\, e^{-[A(t) * F_{batch}(t)] - k_P t - \rho t}\, W(t)\, dt \quad (9).$$

4.2.4 Time Leverage

Equation (9) illustrates that the total revenue, which a semiconductor venture can accrue over its investment horizon, is highly sensitive to the rate at which the various learning efforts proceed. A linear reduction over time of A(t) exponentially increases cumulative revenue (design leverage), as does a linear reduction of batch fault density (quality leverage). However, since batch fault density ($F_{batch}(t)$) itself is an inverse exponential function of the time since venture inception (t), cumulative revenue should be viewed as an exponential function of an exponential function of (t). Furthermore, a drop in fault density triggers the Yield Ramp, during which the wafer output rate grows exponentially as a function of time by an order of magnitude (volume leverage). The exponentially decaying nominal price erosion rate (determined by k_P) and the continuously compounded discount rate (ρ), which reflect time-to-market pressure, give a microprocessor manufacturer an additional incentive to produce at high volumes while the unit product price is high. Consequently, the ability to accrue revenue is *time leveraged:* a slight acceleration of the process development effort can generate a windfall; a slight delay would result in a significant unrealized gain.

4.2.5 Financial Baseline Conditions and the Financial Lifecycle

Figure 2 shows how cash outlays, revenue and profit of a semiconductor venture accrue over the lifecycle of a technology generation. In addition to the manufacturing baseline conditions outlined in section 4.1.4, figure 2 is based up the following financial assumptions, henceforth termed *financial baseline conditions*, which are consistent with what a manufacturer of microprocessors that is not the market leader can expect. Firstly, prices of microprocessors erode according to equation (6), from a level of $10,000 at a rate of 2.75 years per order of magnitude (k_P=0.837). The financial model also assumes an effective cost-of-capital rate of 0.20 or 20% per year for a manufacturer of microprocessors that is not the market leader. Substituting this value into equation (7) results in a continuously compounded discount rate of 0.182. Unless otherwise stated, all financial variables are set to financial baseline conditions from this point on.

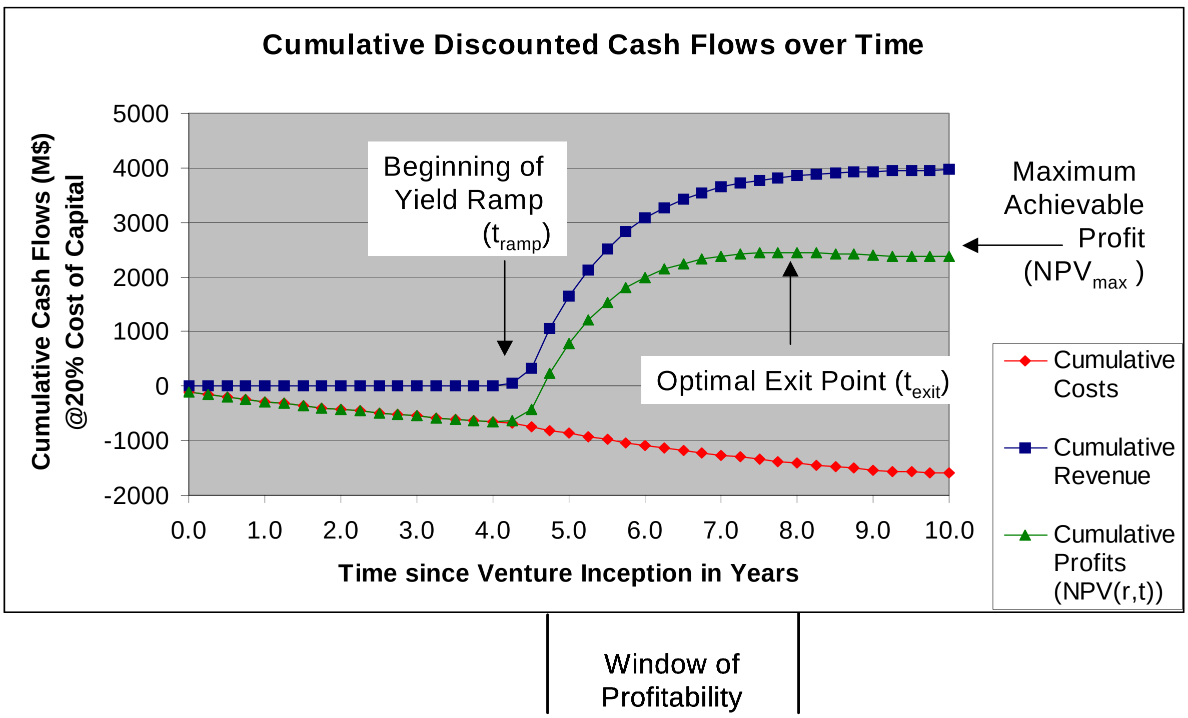

Figure 2: **Discounted cumulative cash flows of a semiconductor venture under baseline conditions for microprocessor manufacturing.**

The three trajectories in Figure 2 depict the cumulative revenues, the cumulative cash outlays and the cumulative profit (Net Present Value), as given by equation (8). For the first four years of the lifecycle the microprocessor manufacturer invests in research, process development and product design, as well as making a concerted effort at integrating technologies developed by outsiders (Iansiti & West, 1997). If all these endeavors are successful, then fault density drops, and yield surges, triggering the Yield Ramp. The semiconductor venture becomes highly profitable during the yield ramp, because the manufacturer is still operating in an environment of capacity constraint that allows him/her to charge a premium price for the manufactured goods. The resulting surge in revenue significantly outweighs the increase in operating costs that is associated with generating said revenues. However, the price drops as the capacity constraint eases; more than 80% of the ventures total profits are accrued within two years of the start of the Yield Ramp. Profitability deteriorates thereafter. The manufacturer should exit the venture at the point of highest level of cumulative profit, which is represented by the highest point of an NPV trajectory (NPV_{max}) and occurs 7.9 years into the venture (t_{exit} = 7.9 years). However, the amortization of capital equipment, which tends to continue beyond the optimal exit point, may deceive the microprocessor manufacturer into persisting with the production of microprocessors at loss rates that may be too small to be noticed.

5. VARYING PARAMETERS

Having established baseline conditions for the Microprocessor Profitability Model, we are now in a position to proceed with identifying the high leverage variables that govern profitability in semiconductor manufacturing by varying the individual parameters of the model, *ceteris paribus*, and displaying the effect on profitability in tabular form (see table 3). Each set of input parameters that is entered into the Microprocessor Profitability Model generates an NPV trajectory such as the one that is displayed in figure 2. The highest value of a particular NPV trajectory (NPV_{max}) represents the maximum cumulative discounted profit that can be expected from the venture under a particular set of conditions. NPV_{max} will diverge from its baseline value in figure 2 when an input parameter to the Semiconductor Productivity Model deviates from baseline conditions. Thus NPV_{max} is an indicator of the performance response to any particular change to baseline conditions, be they induced by an investment in learning or by other factors. A rapid rate of change in NPV_{max} in response to a particular investment in learning may therefore indicate that the particular investment possesses high learning leverage.

Table 3: Learning Rate Acceleration, Quality Leverage, Volume Leverage, Design Leverage and their Effects on Profitability

a) Time Leverage -- Varying the Date of the Yield Ramp					
Start of Yield Ramp (years since venture inception)	3.75	4.25	4.75	5.25	5.75
NPV_{max} (Billions of $)	5.14	2.50	0.91	0.00	0.00
t_{exit} (years since venture inception)	7.9	7.9	7.9	0.0	0.0
b) Quality Leverage -- Varying the Terminal Batch Fault Density					
Terminal Batch Fault Density (Faults/cm^{-2})	0.01	0.03	0.10	0.30	1.00
NPV_{max} (Billions of $)	2.50	2.50	2.49	1.85	0.00
t_{exit} (years since venture inception)	7.9	7.9	7.7	7.4	0.0
c) Volume Leverage -- Adding Capacity					
Date at which Ramp Stops (years since venture inception)	4.75	5.25	5.75	6.25	6.75
Ultimate Wafer Output Rate (1000 wafers per quarter)	900	1800	2700	3600	4500
NPV_{max} (Billions of $)	2.50	4.26	5.24	5.76	5.91
t_{exit} (years since venture inception)	7.9	7.9	7.9	7.9	7.9
d) Design Leverage -- Shrinking the Critical Area					
Date of Design Shrink (years since venture inception)	4.0	5.0	6.0	7.0	8.0
A(r) Critical Area (cm^{-2})	1.41	1.19	1.00	0.84	0.71
Chips per Wafer	141	168	200	238	283
NPV_{max} (Billions of $)	2.50	2.95	3.14	3.21	3.23
t_{exit} (years since venture inception)	7.9	8.1	8.4	8.7	9.8

5.1 Accelerating the Learning Rate

Varying t_{ramp}, the start date of the Yield Ramp, *ceteris paribus*, demonstrates *time leverage:* investments move up t_{ramp} can have a profound impact on profitability. Table 3a shows that bringing the date of the Yield Ramp forward by six months, which corresponds to a learning-rate acceleration of about 12%, more than doubles the NPV_{max} of a microprocessor manufacturing venture, whereas delaying it by six months eliminates two thirds of the expected profit. These figures translate into a cost of about $5000 for every minute of process development time. Thus a problem that is on the critical path of process development can induce a loss rate of $5000 per minute or more. Microprocessor manufacturing ventures that are a year late tend to lose money. NPV_{max} equals zero, and t_{exit} equals zero when t_{ramp} is greater than or equal to 5.25 years because a semiconductor venture that gets delayed by a year or more is one that should not have been begun. Thus for a learning effort in microprocessor manufacturing to be successful, learning must not just occur; it must occur on time or ahead of schedule.

5.2 Factors that Exhibit Diminishing Returns

Tables 3b, 3c and 3d show that the effects on NPV_{max} of quality leverage, volume leverage and design leverage are more limited than the effect of accelerating the learning rate. Varying the terminal fault density of a semiconductor manufacturing process (table 3b) indicates that achieving profitability is difficult at fault densities of 1.0 fault per square centimeter, even for microprocessors, which command a relatively high market price for an integrated circuit product. Quality leverage is very high between 1 and 0.3 faults per square centimeter, a domain that is still governed by the reduction of systematic process faults. In this quality domain, a constant, sustained fault reduction effort that proceeds according to the Pareto Principle reduces fault density at a rate of an order of magnitude per 6-month period (see figure 1), which adds an expected $1.85 billion to the bottom line (see table 3b). Fault density reduction efforts stay ahead of product price erosion during the quality domain in which random fault detection until the reach diminishing returns between 0.1 and 0.03 faults per square centimeters, a quality band that 27 out of 29 responding semiconductor yield management experts in this study considered the state of the art in 2002.

Table 3c looks into the consequences of continuing to ramp wafer output rate beyond baseline conditions. The manufacturer begins the yield ramp at t_{ramp} = 4.25, and continues to add 90,000 wafers per quarter of fab capacity every six months, *ceteris paribus*, a rate of increase that the semiconductor manufacturing experts that have been interviewed for the purpose of this study consider a practical maximum. Table 3c depicts five levels of ultimate capacity, at which a firm that produces microprocessors decides to quit ramping, and the time at which the ramp stops. The price of microprocessors is deteriorating according to baseline conditions while the firm is ramping, and this product price erosion overwhelms any impact that is achieved by economies of scale. Table 3c illustrates that volume leverage reaches diminishing returns. NPV_{max} saturates 7.9 years after the venture inception and begins to decrease thereafter, even if the W(t) continues to be increased at its maximum achievable rate.

Table 3d assumes that a manufacturers of microprocessors generates a new design revision of its product. This design revision replaces the existing revision in the factory one quarter after the new revision becomes available. Each revision contains 15% less critical area A(t) than the previous revision. Table 3d illustrates that annual shrinks of 15% can add up to $0.8 billion in cumulative profits to a semiconductor technology node, more than 85% of which result from the first two shrinks. Therefore, increasing a design's resilience to faults (design leverage) reaches diminishing returns. However, increased resilience pushes out the optimal venture exit time (t_{exit}), extending the market window of the design.

5.3 Platform Leadership and Exogenous Influences

Gawer and Cusumano (2002) have shown that companies who are in a dominant market position *learn* the ability to strategically orchestrate, encourage and coordinate complementary innovation. The additional demand for products that is created by such platform leadership could ameliorate unit price erosion, which can generate significant additional revenues for the dominant market leader. Gawer (2000) has documented that Intel Corporation, the only company in the semiconductor industry that is in a position to exercise such platform leadership, has learned to influence the direction of development of other products by a large number of third parties in the computer industry. Intel's activities could create additional demand for personal computers, which would stimulate demand for microprocessors, Intel's flagship product line. As a result, the unit price for microprocessors may deteriorate at a slower rate than expected, potentially yielding a windfall for Intel.

Table 4: The Effect of Platform Leadership

Rate of Product Price Erosion (years per order of magnitude)	3.50	3.25	3.00	2.75	2.50	2.25	2.00
Decay Constant (k_P) (years^{-1})	0.66	0.71	0.77	0.84	0.92	1.02	1.15
NPV_{max} (Billions of $)	9.42	6.66	4.33	2.50	1.12	0.17	0.00
t_{exit} (years since venture inception)	10.0	10.0	8.6	7.9	7.1	6.3	0.0

According to table 4, in which unit product price erosion is varied, *ceteris paribus*, a market leader such as Intel would have a strong incentive to exercise platform leadership. Reducing the rate of product price erosion from 2.75 to 3.00 years per order of magnitude, an improvement of less than 10%, increases NPV_{max} from 2.50 billion to 4.33 billion, a factor of 73%, and adds about seven months to the window of profitability. Conversely, an uncontrollable exogenous environmental shift (e.g. Freeman & Boeker, 1984; Hannan & Freeman, 1989) that accelerates the rate of price erosion by 10% would cut expected profits by 55%, and a 20% acceleration of the erosion rate would all but eliminate them, implying that highly time-leveraged ventures are highly vulnerable to outside influences.

6. Conclusions and Discussion

Three key findings of this study illustrate how learning in a high technology environment like microprocessor manufacturing differs from what is described in traditional organizational learning theories such as 'learning by doing' or the learning curve. *Firstly*, qualitative evidence from this study suggests that practitioners do not utilize global financial metrics in their learning endeavors. Fault density, critical area and wafer output rate respectively act as performance metrics for quality learning, design learning and volume learning. None of these performance metrics reflect cost or revenue, yet they act as factors that contribute to a microprocessor-manufacturing venture's global financial performance. The magnitude of these factors varies over time, indicating that their relative impact on global financial performance varies over time.

Secondly, the empirically grounded model of the lifecycle of a microprocessor-manufacturing venture, such as the one presented in this paper, indicates that organizational learning in a microprocessor-manufacturing venture can be leveraged to cope with time-to-market pressure. Prolonged, sustained investments in learning at a relatively constant level generate highly non-linear surges in financial performance, but financial performance deteriorates as market windows draw to a close. Contrary to what is stated in the more traditional learning theories, the findings of this study suggest that learning contains a revenue component, as well as a cost component. In addition, under time-to-market pressure, the timing of performance can matter profoundly: *learning* how to produce a few chips when prices are high, can be more important than manufacturing many chips when prices are low.

Thirdly, and perhaps most importantly, varying key parameters of the model, *ceteris paribus*, indicates that a slight, but coordinated acceleration of the organizational learning rate enhances profitability more than any other factor does. Efforts that focus on maximizing product quality, increasing scale or reducing a product's susceptibility to quality problems are subordinate to accelerating the learning rate, and they reach diminishing returns. Time leverage in microprocessor manufacturing is more important than quality leverage, volume leverage or design leverage. A select few firms, which are in a position to exercise *platform leadership* (Gawer & Cusumano, 2002), can leverage time and increase a microprocessor-manufacturing venture's profitability by delaying product price erosion.

A series of studies, which have used the semiconductor industry as a setting, have elucidated many of the mechanisms that enable semiconductor manufacturers to accelerate their organizational learning rates. For example, Iansiti & West (1997) report that complex semiconductor manufacturing processes are integrated from constituent technologies, which are developed by suppliers that have accumulated expertise in a variety of scientific disciplines. Thomke (1998) documents how extensive simulation activity gives way to physical experimentation, once the latter learning mechanism provides more quality leverage than the former does. Terwiesch & Bohn (2001) investigate how learning and increasing scale occur concurrently in a ramp-up to production. They observe a series of tradeoffs between quality and the number of products started per unit time, and conclude that earlier learning is more valuable than later learning during a ramp-up, even if product prices are high and experiments create a large opportunity cost. Hatch & Mowery (1998) have shown that technology transfers from R&D laboratories to volume production facilities can adversely affect the batch yield of mature semiconductor processes, which run in the volume production facilities prior to the transfer. Weber (2002) concluded that problem solving under time pressure increases the cost of knowledge transfer by concentrating disciplinary knowledge within the minds of experts, which results in competitive advantage for firms that can retain or provide continuous access to experts in a wide variety of disciplines. Gawer (2000) details how Intel, which is in a dominant market position in microprocessor manufacturing, can stimulate demand for its products through platform leadership. In aggregation, these studies suggest that developing a time-leverage capability constitutes a complex coordination problem requiring a high level of management skills in human resources, technology and finance, a high-wire act that is sufficiently rare, so as to comprise a significant barrier to entry.

A series of studies in the automobile industry (Clark & Fujimoto, 1991; Womack, Jones & Roos, 1991; and Cusumano & Nobeoka, 1992), in which unit price tends to deteriorate as new models arrive on the market, suggest that learning leverage under time-to-market pressure is not restricted to high technology environments. The findings of these studies demonstrate that shorter product life cycles allow firms to replace and add models more quickly, which gives them wider market coverage and potentially larger market share. Rapidly moving firms also tend to be more flexible than their slower competitors, allowing them to react to market shifts more swiftly and integrate technology at a more rapid rate. The production skills from which such firm agility is derived can result from leveraged learning practices. For example, Nobeoka & Cusumano, (1997) have shown that many of the lessons of designing one particular type of automobile are passed on to the next model, sometimes before the first model goes into production. In addition, learning leverage under time-to-market pressure is not unique manufacturing. For example, Cusumano and Selby (1995) have observed software designers at Microsoft bin errors into four categories of estimated economic severity. Errors of severity 1 cause the product to halt and must therefore be found, whereas errors of severity 4 are minor, making their elimination of lower economic significance. Learning leverage is obtained through corrective action, which is taken according to the Pareto Principle. Just like in microprocessor manufacturing, the ostensibly worst errors are attacked first, even though the impact of these errors on the bottom line cannot necessarily be quantified precisely.

Expanding organizational learning theory to cover learning leverage under time-to-market pressure in the variety of environments in which it occurs, may yield ample opportunity for academic study. For example, how the learning efforts of highly differentiated organizational subsystems (e.g. sales, marketing, R&D, process engineering, operations or equipment maintenance) are unified to accomplish the tasks that the organization as a whole desires to achieve (Lawrence & Lorsch, 1967) in an *accelerated* and *leveraged* manner remains largely unanswered. In addition, the management literature does not yet contain studies that describe how learning at the level of constituent technologies is amalgamated into a global learning effort, a prerequisite capability for integrating constituent technologies into a sophisticated high tech industrial process (Iansiti & West, 1997). Finally, the nature of the relationships between the Pareto-driven problem-solving practices of high technology organizations and high-level financial metrics such as Net Present Value has not yet been characterized completely. The author of this paper is currently conducting research in all these areas, because he believes the above subjects could constitute topics of potential interest to practicing high technology managers that strive to achieve competitive advantage through the acquisition of knowledge, as well as to academic scholars who explore how competitive advantage through organizational learning is derived.

APPENDIX A: DETAILS OF EMPIRICAL STUDY

The Microprocessor Profitability Model is based on projections of technical trends, which are published in the Semiconductor Industry Association's 2001 edition of the International Technology Roadmap for Semiconductors (SIA-ITRS). The technology generation under investigation is the 130-nanometer[xv] (130-nm) technology node, the latest generation to go into production in 2002. The assumptions for defect density trends come from two primary sources:

the UC Berkeley study that benchmarked best practices across the semiconductor industry (Leachman 1996; Leachman and Hodges, 1996) and 25 years of fault density trend data from IBM (Stapper, 1995). The chip price profile is extrapolated from Moore's Law (Moore, 1975), which has characterized the reduction of integrated circuit prices and feature sizes since the 1960s. It is consistent with the 350-nm, 250-nm and 180-nm and 130-nm technology nodes, which have successively dominated semiconductor manufacturing between 1995 and 2002.

I had to conduct 90 personal, one-on-one interviews to interpret the defect density trend data, in a manner that I believe leads to correct conclusions. The UC Berkeley study (Leachman, 1996; Leachman & Hodges, 1996) was completed in 1996, when 350-nm technology was in early volume production at most leading edge manufacturers. Personal interviews confirmed the repetition of the observed fault density patterns for the 250-nm technology node in the 1997-2002 timeframe, and achieved near consensus values for 180-nm technology. Interviews achieved the same for the data from IBM (Stapper & Rosner, 1995) and HP (Weber, Moslehi & Dutta, 1995), which are normalized for reasons of confidentiality. A reasonable assessment of the actual fault densities of the IBM dataset, and the HP dataset, as well as projections for 130-nm technology, are the result of a series of interviews of yield engineers, yield managers, and yield analysts that work for/with microprocessor manufacturers or suppliers of inspection/metrology tools. Semiconductor R&D managers and manufacturing managers assisted in the assessment of the cost side of semiconductor ventures. Managers from companies that produce microprocessors as well as purchasing managers and analysts that work for the customers of microprocessor manufacturers made estimates of the unit price of microprocessors.

The abovementioned diversity of respondents poses a limitation on the methodology that has been deployed in this paper. Completing a task as complex as semiconductor process development requires a significant amount of knowledge that is differentiated with respect to relevant external environment of the various organizational subsystems (e.g. sales, marketing, finance, research, production, process engineering, and maintenance), and the differentiated knowledge of the various subsystems must be integrated to achieve unity of effort for the organization as a whole (Lawrence & Lorsch, 1967). Analogously, a semiconductor manufacturing process is integrated from a diverse set of constituent technologies (e.g. lithography, vacuum systems, gas plasmas, chemical vapor deposition) that are derived from a diverse set of scientific disciplines (Iansiti & West, 1997), knowledge of which is not necessarily common to many experts in the semiconductor industry (Weber, 2002). Thus experts associated with a particular organizational subsystem or technology may not be qualified to comment on the activities and environments of other organizational subsystems or about technologies at which he/she is not considered an expert. Questions pertaining to specific subsystems, environments and technologies were thus directed to respondents who had been recommended as experts in a specific field by at least two of their peers. The complexity of semiconductor manufacturing and process development, as well as the supply and demand chains associated with these activities, limited the number of qualified respondents to a minimum of four for some questions and a maximum of 30 for others. Since the majority of posited questions had to be answered to construct the Microprocessor Profitability Model, some of the conclusions upon which this model is based may not be statistically significant. Instead, the Microprocessor Profitability Model reflects the consensus opinion of top experts in the semiconductor industry. Its conclusions are likely to be more than reasonable estimates of expected values, but standard deviations or other measures of variability have been difficult to determine. Issues regarding the variability of the model's key parameters are instead explored by varying these parameters, *ceteris paribus*.

The 69 cases of solved and unsolved semiconductor manufacturing and process development problems were collected establish a correspondence between how individual problems are solved and how an organization learns. The cases span the last quarter of the 20th century, and they involve a total of 35 microprocessor manufacturers in Asia, Europe and North America, as well as 23 firms that supply process and diagnostic technology to the semiconductor industry. The various cases in the sample cover semiconductor processes at all levels of maturity, from early research to mature volume production, a feature of the data set that may help reveal conditions and learning modes that are specific to particular levels of process maturity.[xvi]

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[i] VanBree's (1995) study of semiconductor economics has shown that the demand for semiconductor products creates a "bullwhip effect" (Sterman, 1989; Lee et al., 1997) in the semiconductor industry in which the suppliers of technology are exposed to a more volatile economic environment than their customers are. VanBree (1995) argues that the demand for microprocessors drives the demand for memory chips and many application-specific integrated circuits. The price of microprocessors is thus less volatile than that of these other integrated circuits.

[ii] The traditional learning curve (e.g. Argote & Epple, 1990) can be expressed as the power function $C_n = a\,n^{-b}$, where "n" stands for the cumulative number of units produced, C_n denotes the cost of the n^{th} unit, and "a" is the cost of the first unit produced. The parameter "b" represents the learning elasticity, which measures the rate at which labor hours are reduced as cumulative output increases. Both a and b are constants; $a > 0$; and if the organization is learning more than it is forgetting, then $0 \leq b \leq 1$. The parameter "n" reflects the investment in learning, whereas C_n gives the return on the learning investment. The experience curve, a cousin of the learning curve, frequently uses average total cost (ATC) as a performance metric. The average total cost is given by ATC = TC/n, where n denotes the number of units that have been sold at a given point in time, and TC represents the total costs, fixed and variable, that a firm has accumulated when the n^{th} unit is sold (Maital, 1994, p. 139). Learning curves can also be expressed in terms of their progress ratio (p), which is given as $p = 2^{-b}$, where p denotes the fraction of the unit cost that results from a doubling in cumulative output (e.g. Argote & Epple, 1990). Arrow's (1962) definition of learning by doing uses cumulative investment rather than cumulative output as the independent learning variable.

[iii] Data from Hirsch (1956) and Fellner (1969) allowed Dudley (1972) to distinguish between simple learning processes, in which learning occurs through the repetition of the same physical task, and complex processes that require learning how to learn. Dudley (1972) argues that learning to perform simple tasks such as assembly and repair would be output dependent, whereas learning how to execute tasks that involve complex operations such as metal working, casting, forging and stamping is probably time dependent.

[iv] Semiconductor Industry Association, The International Technology Roadmap for Semiconductors, 2001

[v] Semiconductor products by nature are very flat rectangular prisms whose depth is determined by the standardized thickness of silicon wafers. Certain areas of a chip are susceptible to faults, whereas others are not. For issues related to determining the critical area of semiconductor integrated circuits see, for example, A. V. Ferris-Prabhu, "The role of defect size distribution in yield modeling," *IEEE Transactions on Electron Devices*, Vol. ED-32 (9), pp. 1727-1734, 1985; A.V. Ferris-Prabhu, "Modeling of Critical Area in Yield Forecasts", *Journal of Solid-State Circuits*, SC-20(4), pp. 878-880; H. Walker, "VLASIC: A catastrophic fault yield simulator for integrated circuits", *IEEE Trans. Comp. Aided Design*, vol. CAD-5, pp. 541-556, Oct 1986; G.A. Allan and A.J. Walton, "Efficient Critical Area Algorithms and Their Application to Yield Improvement and Test Strategies", *1994 IEEE International Workshop on Defect and Fault Tolerance in VLSI Systems*, pp. 88-96, Montreal, 17-19th Oct 1994; and P.K. Nag and W. Maly, "Hierarchical extraction of critical area for shorts in very large scale ICs", *IEEE Workshop on Defect and Fault Tolerance in VLSI Systems*, pp. 19-27, Lafayette, Louisiana, Nov 1995.

[vi] While only one fault in a product prevents the product from being sold, a product that cannot be sold may contain multiple faults of different types. Thus the relationship between the number of functioning products in a batch and the number of faults in a batch is inherently non-linear. Equation (1), which is known as the Poisson yield model, assumes an even distribution of faults within a batch (wafer). For alternative relationships between batch yield and the number of faults per batch, which assume fault clustering or other inhomogeneities, please see C. Stapper, "Modeling of integrated circuit defect sensitivities," *IBM J. Res. Develop*., vol. 27, pp. 549-557, Nov. 1983; or J. Cunningham, "The use and evaluation of yield models in integrated circuit manufacturing," *IEEE Trans. Semicond. Manufact*., Vol. 3, no. 2, pp. 60-71, May 1990.

[vii] Batch yield is also known as die-sort yield or chip yield in the semiconductor industry.

[viii] When the batch yield of state-of-the-art integrated circuit products is extremely low, these products cannot be used to conduct statistically significant fault-reduction experiments. (Please see U. Kaempf, "Statistical significance of defect density estimates," *IEEE/ICMTS*, 1988, pp 107-113.) Semiconductor manufacturers try to circumvent this problem by designing "dummy products", which are appropriately sized to conduct statistically significant experiments and stress circuit features that are expected to be particularly vulnerable to known fault mechanisms.

(Please see, for example, E. J. Sprogis and R. E. Newhardt, “Defect Diagnostic Matrix – A defect-learning vehicle for submicron technologies,” *Proc. IEEE/ICMTS*, 1988, pp. 103-106.)

[ix] For a listing and description of key activities that concern semiconductor process development, please see Y. Nishi, “VLSI research and development in the US and Japan,” *Proc. Mat. Res. Symp. VLSI* V, 1990, pp. 3-11.
[x] For a discussion of statistics pertaining to wafer-to-wafer yield variation, please see U. Kaempf, “The binomial test: A simple tool to identify process problems,” *IEEE Trans. Semicond. Manufact.*, Vol. 8, no. 2, May 1995, pp. 160-166.

[xi] Cost of Ownership (CoO) models strongly influence financing decisions, purchasing decisions and manufacturing practices in the semiconductor industry. For a description of the line of reasoning behind CoO models please see R. Carnes and M. Su, "Long term Cost of Ownership," *IEEE/SEMI Int'l Manuf. Sci. Symp.* 1991, pp. 39-43; R. Martinez, V. Czitrom, N. Pierce and S. Srodes, "A methodology for optimizing Cost of Ownership," *SPIE* Vol. 1803 (1992) pp. 363-387; J. Secrest and P. Burggraaf, "The reasoning behind Cost of Ownership*," Semiconductor International*, May 1993; R. Doering, "Cost-of-Ownership issues in a flexible manufacturing environment*," Solid State Technology*, Feb. 1994, pp. 39-43; D. Dance and D. Jimenez, "Applications of Cost of Ownership," *Semiconductor International*, Sept.1994, pp. 6-7.

[xii] It should be noted that the definition of C(t) assumes that production costs are independent of product, an assumption that is valid as long as all integrated circuits in a factory are realized by one manufacturing process. However, the financial model of the semiconductor lifecycle does not assume product independence for revenues. Instead, it assumes that a fab that could make a plethora of products with different pricing functions has chosen to manufacture only one – a state-of-the-art microprocessor.

[xiii] For more details on the evolution of memory pricing, please see Y. Tarui & T. Tarui, “New DRAM pricing trends: The bi-rule,” *IEEE Circuits and Devices Magazine*, March 1991 vol. 7, no. 2, pp. 44-45.

[xiv] Please see G. Moore, “Progress in digital integrated circuits,” *IEDM Tech. Dig*., 1975, p. 11. The cost per bit of memory and the size of integrated circuit have been shrinking by a factor of four about every 30 months since about 1965.

[xv] A technology node is defined by the smallest feature on an integrated circuit that can be fabricated by a process of that generation. A process of the 130-nanometer technology node or generation can therefore successfully produce integrated circuits that contain features whose widths are as small as 130 nanometers.